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A SAR-ADC using unit bridge capacitor and with calibration for the front-end electronics of PET imaging

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ABSTRACT

This paper presents a 12-bit 1 MS/s successive approximation register-analog to digital converter (SAR-ADC) for the 32-channel front-end electronics of CZT-based PET imaging system. To reduce the capacitance mismatch, instead of the fractional capacitor, the unit capacitor is used as the bridge capacitor in the split-capacitor digital to analog converter (DAC) circuit. In addition, in order to eliminate the periodical DNL errors of −1 LSB which often exists in the SAR-ADC using the charge-redistributed DAC, a calibration algorithm is proposed and verified by the experiments. The proposed 12-bit 1 MS/s SAR-ADC is designed and implemented using a 0.35 μm CMOS technology, it occupies only an active area of $986 \times 956\ \mu m^2$. The measurement results show that, at the power supply of 3.3/5.0 V and the sampling rate of 1 MS/s, the ADC with calibration has a signal-to-noise-and-distortion ratio (SINAD) of 67.98 dB, the power dissipation of 5 mW, and a figure of merit (FOM) of 2.44 pJ/conv.-step. This ADC is with the features of high accuracy, low power and small layout area, it is especially suitable to the one-chip integration of the front-end readout electronics.

1. Introduction

The Positron Emission Tomography (PET) imaging system is a noninvasive molecule-level imaging technique which allows clinical diagnosis by measurement of the metabolic activity. The measurement principle is based on the detection of γ-ray radiations resulting from the disintegration of positrons emitted by the radiotracer [1]. As shown in Fig. 1, after a radioactive tracer is injected into the blood circulation, the annihilation caused by the combination of a positron emitting from the radiotracer and an electron from the biology organism leads to generation of two γ-photons. These two γ-photons have the energy of 511 keV, emit in the opposite direction, and finally reach to the detectors. The areas with high concentration of radioactive tracer are detected with a scanner after data processing, thus the lesion areas of the biology organism can be located.

Cadmium Zinc Telluride (CZT) detectors [2] have high energy resolution and can work at the room-temperature, they will be one of the principal detectors for the next-generation PET imaging systems.

For the small-animal PET imaging, application specific integrated circuits (ASICs) are commonly used to reduce the volume and power dissipation of the front-end electronics, and it is necessary to design the fully-customized readout ASICs to meet the characteristics of CZT detector modules and the specifications of the PET imaging systems.

The typical 32-channel CZT detector PET imaging system, as shown in Fig. 2, consists of CZT detectors, the front-end electronics including the front-end readout chip and ADC chip, a digital signal processor (DSP) and an image-reconstruction platform such as workstation or PCs. The front-end electronics together with the detectors convert the deposited energy of the particles to the digital signals. These digital signals are then processed by the digital signal processor (DSP) for the preliminary data processing, and the image-reconstruction will be completed by a PC.

The front-end readout chip contains 32 channels of front-end readout chain, and each front-end readout chain is mainly composed of a charge sensitive amplifier (CSA), a pulse shaper (PS), a peak detect-and-hold circuit (PDH), and an output buffer. The weak current signals from the CZT detectors are read out by a CSA which is followed by a pulse shaper to improve the signal to noise ratio (SNR). The peak value of the shaped pulse is detected and held by PDH, which is followed by an output buffer to isolate the following circuits. The peak voltages of 32 channels are sampled and digitalized in sequence by a high-speed and high-resolution ADC.

It is desired to integrate the front-end readout circuits and ADC on one chip for shrinking the volume of the front-end electronics. However, considering the low-noise performance required for the front-end readout system, the front-end readout circuits and ADC are realized by separate chips on the first step. In this paper only the

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design and measurement of the ADC chip are considered, which will be integrated with the front-end readout circuits in the near future.

For the multi-channel front-end electronics of PET imaging system, SAR-ADC is particularly suitable for its outstanding characteristics of low power, small die size and reasonable converting speed and resolution. For the CZT detector-based small animal PET imaging system, the highest count rate of γ-ray for every channel is considered to be 10 k per second [3]. For the 32-channel front-end readout circuits equipped with only one ADC, the sampling time period of ADC is about 3 μs, namely the ADC's sampling rate must be up to 0.3 MS/s, so the ADC's sampling rate is set to be 1 MS/s in this design. Besides, In order to match with the front-end readout circuits, the other features of ADC are decided as: the resolution is 12-bits, and the reference voltage is 4.096 V.

2. Proposed SAR-ADC

Previously we have designed a 12-bit SAR-ADC chip which is aimed to use in the front-end electronics of CZT detector-based gamma spectrometer [4]. For this SAR-ADC, since a hybrid 12-bit DAC consisting of 6-bit charge-redistribution DAC (CDAC) and 6-bit resistor-string DAC (RDAC) was used, it obtained the higher accuracy at the sacrifice of the power and die size. For the multi-channel front-end electronics of PET imaging system, however, the power dissipation and die size are the priority performances, so the CDAC should be only used in the SAR-ADC, because the RDAC not only consumes quiescent current but also takes large layout area.

The binary-weighted CDAC was widely used in the SAR-ADC. However, due to the maximum capacitance value of the CDAC array increases exponentially with the resolution of ADC, the capacitance values are with large distribution, which will degrade the performances of SAR-ADC, such as the power dissipation and converting time are all increased because the larger the capacitors the larger the charging or discharging currents and the settling time. Besides, the layout area is also increased, and the converting accuracy becomes worse because the matching of the capacitance values is difficult for the large distribution of capacitance values.

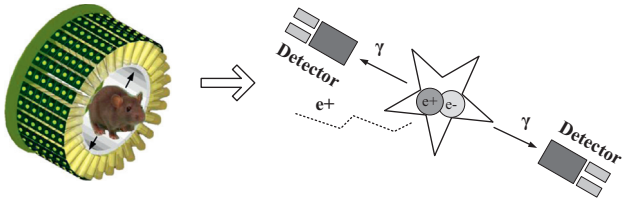

Fig. 1. Principle of PET imaging.

The split-capacitor CDAC can be used to overcome above issues existing in the binary-weighted CDAC [5]. A 12-bit SAR-ADC using the split-capacitor CDAC is shown in Fig. 3, in which a 12-bit binary-weighted capacitor array is split into two 6-bit capacitor arrays (LSB array and MSB array) by using a bridge capacitor C_b, and the capacitance values distribution is significantly reduced from $C\sim2048C$ $(=2^{11}C)$ to $C\sim32\,C$ $(=2^5C)$. However, since the total weight of the LSB array should be equal to the weight of the lowest bit in the MSB array, a fractional bridge capacitor C_b is needed which has the capacitance value of $(64/63)C$. Because the fractional bridge capacitor has the poor matching with other integer capacitors, the converting accuracy of ADC will be degraded.

In order to resolve the poor matching problem of the fractional bridge capacitor, the unit bridge capacitor can be used [6,7]. Fig. 4 shows a 12-bit SAR-ADC designed this work, in which the split-capacitor CDAC with a unit bridge capacitor is adopted to improve the matching of capacitances, and in addition, the fully differential architecture is used to eliminate the effects of the noise from both the substrate and the power supply. The operation of the SAR-ADC shown in Fig. 4 is divided into two modes: sample mode and conversion mode, the detail operation principal is analyzed below.

2.1. Sample mode

In Fig. 4, in the sample mode, the switches of *SP7*∼*SP13* and *SN7*∼*SN13* are connected to V_{INP} and V_{INN}, respectively, the two inputs of comparator are reset to V_{CM}, and the switches of *SP1*∼*SP6* and *SN1*∼*SN6* are connected to 0 and V_{REF}, respectively. The equivalent circuit in the sample mode is shown in Fig. 5. The total charge at the positive and negative input of comparator, Q_P and Q_N, can be expressed as Eq. (1) and Eq. (2), and the differential input V_{IN} is defined as Eq. (3).

$$Q_P = 64C \times (V_{INP} - V_{CM}) + (63C//C)(0 - V_{CM}) \quad (1)$$

$$Q_N = 64C \times (V_{INN} - V_{CM}) + (63C//C)(V_{REF} - V_{CM}) \quad (2)$$

$$V_{IN} = V_{INP} - V_{INN} \quad (3)$$

2.2. Conversion mode

The equivalent circuit in the conversion mode is shown in Fig. 6, where C_1, C_2, C_3 and C_4 are the total capacitance connected to V_{REF} or 0 in the CDAC array, which can be calculated using Eq.

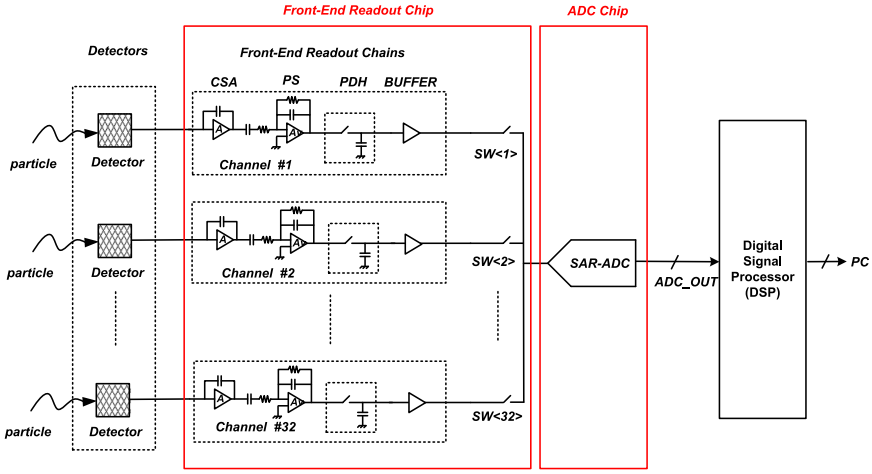

Fig. 2. Block diagram of typical 32-channel CZT detector PET imaging system.