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Radiation hardness of a 180 nm SOI monolithic active pixel sensor

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ABSTRACT

The use of Silicon-on-Insulator (SOI) technology as a particle detector in a high radiation environment is, at present, limited mostly by radiation effects on the transistor characteristics, back gate effect, and mutual coupling between the Buried Oxide (BOX) and the sensor. We have fabricated and tested a new 0.18 μm SOI CMOS monolithic pixel sensor using the XFAB process. In contrast to the most commonly used SOI technologies, this particular technology uses partially depleted SOI transistors, offering a double well structure, which shields the thin gate oxide transistors from the BOX. In addition, an increased distance between transistors and a thicker BOX than has been previously used offers promising solutions to the performance limitations mentioned above. The process further allows the use of high voltages (up to 200 V), which are used to partially deplete the substrate. Thus, the newly fabricated device in the XFAB process is especially interesting for applications in extremely high radiation environments, such as LHC experiments. A four stage validation programme of the technology and the fabricated monolithic pixel sensor has been performed and its results are shown in this paper. The first targets radiation hardness of the transistor characteristics up to 700 Mrad, the second investigates the existence of the back gate effect, the third one targets the coupling between the BOX and the sensor, and the fourth investigates the characterization of charge collection in the sensor diode below the BOX.

1. Introduction

Silicon-on-Insulator (SOI) technologies have been developed for military and space applications for 40 years. Nowadays, they are widely used for commercial and industrial production. SOI devices exhibit major advantages over bulk substrates including superior Single Event Upset (SEU) tolerance, better noise isolation, speed and density [1,2]. Using SOI technologies as pixelated particle detectors enable isolating standard CMOS readout electronics from a high resistivity substrate used as a sensor. This would have several advantages [3]. However, there are some performance limitations to be considered. On one hand, the total ionizing dose (TID) response of SOI devices is more complex than bulk silicon devices as the effects in the buried oxide (BOX) need to be considered as well. A significant influence of radiation damage on the transistor characteristics due to the accumulated charges in the BOX has been observed and published in SOI technologies [4,5]. On the other hand, it has been observed that the applied electric field in the sensor also affects the transistors operation, which is called Back Gate Effect [3]. Additionally, a possible coupling between charges accumulated in the BOX and sensor would also need to be taken into account.

A new 0.18 μm SOI CMOS fully monolithic pixel sensor designed by University of Bonn was fabricated using the XFAB process [6]. The first version of this chip, the so-called XTB01, is 300 μm thick, with a size of 5 mm × 2 mm. In contrast to other SOI technologies, XFAB provides a double well structure to shield the thin gate transistors from the BOX. The transistors are partially depleted (PD), but in contrast with standard PD, a larger distance between gate and BOX and a thicker BOX make the technology promising against the radiation effects on the transistors, as well as against the back gate effect described above. The process further allows the use of high bias voltages (HV) up to 200 V. The chip is composed of four matrices with different pixel sizes (25 μm × 25 μm, 50 μm × 50 μm, 50 μm × 50 μm, 100 μm × 100 μm) and test transistors of several flavours. The chip is composed of four HV rings. Three of the HV rings surround the matrices (100 μm × 100 μm matrix, 50 μm × 50 μm and 25 μm × 25 μm+50 μm × 50 μm) while the fourth HV ring surrounds the whole chip. A detailed description of the chip design is given in [7]. A pixel cross-section of this prototype is shown in Fig. 1.

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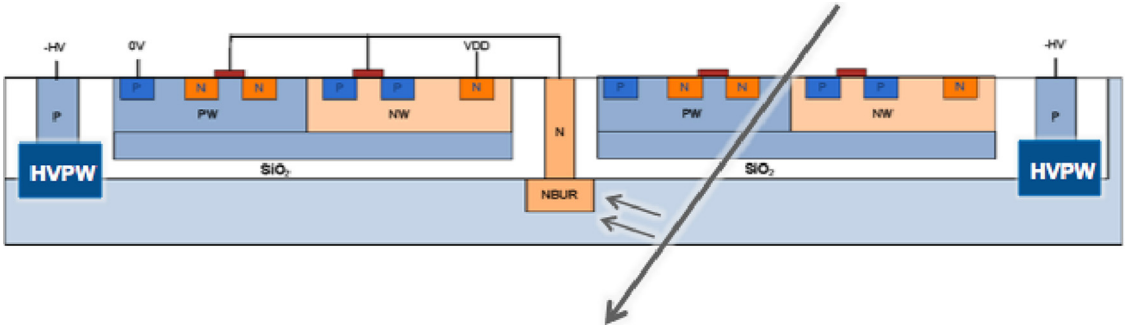

Fig. 1. A pixel cross-section of the XTB01 prototype. Not to scale.

The BOX isolates the full CMOS electronics built in 0.18 μm technology from the substrate which is used as a sensor diode. This substrate is p-type silicon with 100 Ω cm resistivity. The charge is collected in a small deep n-well, which reduces the capacitance, and is connected to the readout circuitry. The HV is applied from the top, on the p+ implants, since there is currently no backside processing. The matrix is read out by a rather simple but slow, standard 3 T pixel cell using a rolling shutter readout for the sensor diode and correlated double sampling [8].

A validation program of the technology and the fabricated monolithic pixel sensor have been carried out a in a four stage approach. The first targets the radiation hardness of the transistor characteristics with focus on possible influences of the BOX. The second stage investigates the existence of the Back Gate Effect. The third targets a possible coupling between BOX and sensor, while the fourth characterizes the leakage current and the charge collection in the sensor diode below the BOX.

2. TID effects on SOI 0.18 μm transistors

Basic TID mechanisms and damage processes in CMOS transistors are described in [9,10]. The electrical parameters of CMOS electronics degrade with accumulated TID due to radiation damage. The shift of the electrical parameters is mainly given by the sum of two contributions, a first one related to the positive charges trapped in the gate and STI oxide and a second one related to the Si–SiO_2 interface traps. The biggest difference between the radiation response of MOS transistors fabricated on bulk silicon and on SOI technology is the BOX inclusion, which make SOI devices more sensitive than bulk transistors to TID damage due to the build-up of charge in the BOX [11,12].

The threshold voltage of a bulk NMOS transistor in the presence of radiation damage is expected to shift in a rebound way. For low TID the trapped positive charges in the gate and STI oxides attract negative charges to the Si–SiO_2 interface and thus decrease the threshold voltage while for high TID the activation of traps at the Si–SiO_2 interface decreases the mobility of the charge carriers which leads to an increase of the threshold value. However, the threshold voltage of a PMOS transistor always tends to increase, because the two effects mentioned above shift the electrical parameters in the same direction. In this case, the positive trapped charges in the oxide push away holes from the p-channel, consequently, increasing the threshold voltage of a PMOS transistor. The leakage current of an NMOS transistor increases with decreasing threshold voltage. The trapped charges in the oxide will provoke an induced negative channel and hence the leakage current increases, while the interface traps will tend to reduce it. For a PMOS transistor, the leakage current is constant. The variation of an induced channel of electrons does not affect a PMOS transistor. The impact of these effects depends on the transistor geometries, for example enclosed transistors are developed to reduce it. The bias conditions of the gate during irradiation are crucial since they will influence the quantity of charges trapped in the Si–SiO_2, the location of the trapped charges, as well as the electrical field at the Si–SiO_2 interface. However for PMOS transistors it is not clear which are best or worst bias conditions, with the result that it is technology dependent.

Table 1
Bias conditions of the transistors gate during irradiation.

Bias conditions	
Campaign A	NMOS on (G=1.8 V, D=S=0 V) PMOS off (G=D=S=1.8 V)
Campaign B	NMOS off (G=D=S=0 V) PMOS on (G=0 V, D=S=1.8 V)

Two irradiation campaigns were carried out at CERN, Switzerland, with an X-ray machine. Irradiations have been performed at room temperature up to a TID of 700 Mrad in several steps with a dose rate of 8 Mrad h^{-1} (achieved by 2 cm tube distance, 40 kV and 50 mA). The dose steps are 100 krad to 600 krad in 100 krad steps, 800 krad, 1 Mrad, 3 Mrad, 5 Mrad, 15 Mrad, 50 Mrad, 100 Mrad, 150 Mrad, 300 Mrad, 500 Mrad, 700 Mrad. The transistors were various types – standard transistors with different geometries and enclosed transistors. Different bias conditions were applied during irradiation for each campaign, since the gate voltage wire bond pad is shared in PMOS and NMOS transistors. The bias conditions during irradiation are summarized in Table 1. The testing procedure followed the Standard test method ESA/SCC BS 22900 [13], in which the transistor characteristics are tested right away after the irradiation step. Therefore, the annealing is considered negligible during irradiation and testing. A full annealing program is performed at the end of the full irradiation campaign. No annealing results are included in this paper.

The setup to characterize the transistors consists of a home-made board which allows selection of every single transistor, and three power supplies (for biasing the gate, drain and AVDD respectively) which allow measuring the transistor characteristics. A dedicated routine extracts the electrical parameters (threshold voltage, leakage current, and transconductance) from the transistor characteristics. The parameter's extraction was based on the extrapolation method in the saturated region (ESR) [14]. Fig. 2 shows the characteristics of the smallest PMOS transistor 0.5/0.18 for all the irradiation steps up to 700 Mrad. This shows how the curve changes under radiation and consequently its electrical parameters.

Fig. 3a and b shows the threshold voltage shift evolution with TID for NMOS transistors of the XTB01 prototype for bias option A (NMOS on) and for bias option B (NMOS OFF) respectively. It is