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ATLAS pixel IBL modules construction experience and developments for future upgrade

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ABSTRACT

The first upgrade of the ATLAS Pixel Detector is the Insertable B-Layer (IBL), installed in May 2014 in the core of ATLAS. Two different silicon sensor technologies, planar n-in-n and 3D, are used. Sensors are connected with the new generation 130 nm IBM CMOS FE-I4 read-out chip via solder bump-bonds. Production quality control tests were set up to verify and rate the performance of the modules before integration into staves. An overview of module design and construction, the quality control results and production yield will be discussed, as well as future developments foreseen for future detector upgrades.

1. Introduction

The Pixel Detector [1] is the innermost component of the ATLAS experiment [2] and it is therefore located very close to the interaction region. The pixel tracking system consists of three concentric barrel layers (with mean radii of 50.5 mm, 88.5 mm and 122.5 mm) and six disk layers, arranged in two endcaps with three disks each. It provides at least three high accuracy space-point measurements per track for pseudo-rapidity $|\eta| \leq 2.5$, as needed for track and vertex determination. The innermost pixel layer (the so-called B-Layer) plays a crucial role for tracking, vertexing, and *b*-tagging capabilities of ATLAS. The Pixel Detector is composed by 1744 modules in total. Each module consists of a $16.4 \times 60.8\ \mathrm{mm}^2$ planar n-in-n silicon sensor tile, 250 μm thick, with 47,232 pixels (size of $50 \times 400\ \mu\mathrm{m}^2$), connected to 16 front-end (FE-I3) integrated circuits. The detector has been designed to face a TID[1] of 50 MRad (expected at 300 fb^{-1}), a NIEL[2] of 1×10^{15} 1 MeV $\mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ and a peak luminosity of $1 \times 10^{34}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}$. Given the present LHC schedule, the peak luminosity should reach $2\text{–}3 \times 10^{34}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}$ in the operation after the 2013–2014 shut-down, thus generating some inefficiency in the B-Layer where the occupancy is higher. For this reason a program of upgrade has been arranged.

2. ATLAS insertable B-layer

The Insertable B-Layer (IBL) [3] is the fourth pixel layer, that has been added to the Pixel Detector between the beam pipe and the B-layer, at a sensor average radius of 33 mm. To make the insertion of the IBL possible, the beam pipe has been replaced by a new one, with reduced radius (from R=29 mm to R=24 mm), built of Beryllium. The IBL consists of 14 staves (64 cm long, 2 cm wide), tilted in ϕ at 14° to guarantee hermeticity and optimize charge collection. Each carbon-fibre IBL stave carries and provides cooling to 32 FE-I4 [4] read-out chips, which are bump-bonded to silicon sensors. In the IBL two different silicon sensor technologies have been used: planar n-in-n and 3D with passing through columns. Each IBL stave is populated with planar pixel technology (12 double chip modules) in the central region and 3D technology (4+4 single chip modules) in forward region.

The IBL has been built to sustain high radiation levels, up to a NIEL of 5×10^{15} 1 MeV $\mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ and a dose of 250 MRad (Fig. 1).

3. Silicon radiation technologies in IBL

3.1. Sensors

The main requirements that IBL sensors have to satisfy are as follows [5]:

1. In order to reduce the material budget the sensor thickness must be between 150 and 250 μm. This will also allow charge

[1] Total Ionizing Dose.

[2] Non-Ioninizing Energy Loss, where 1 MeV n_{eq} is the number of particles with a non-ionizing energy loss of a 1 MeV neutron.

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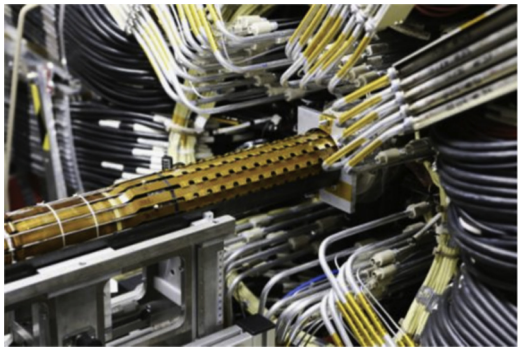

Fig. 1. Insertable B-Layer during its insertion in the ATLAS Pixel Detector.

collection in planar sensors to be more efficient at very large radiation fluences [6].

2. The power dissipation has been required to be lower than 200 mW/cm^2 at the end of life.
3. The maximum leakage current the FE-I4 can compensate is 100 nA/pixel. The sensors had been designed in order not to overcome this value at the maximum expected fluence.
4. The sensor operating temperature is -15 °C or higher at 200 mW/cm^2
5. The in-time hit efficiency is requested to be $>97\%$ at a benchmark fluence of 5×10^{15} n_{eq}/cm^2 and bias voltage lower than 1000 V (for Planars). The specification does not include geometric inefficiencies. This specification is chosen to limit the degraded performance after irradiation.

3.1.1. *Planar sensors*

The devices are produced on n-type, Float Zone (FZ) silicon sensors with ⟨111⟩ crystal orientation and a bulk resistivity of 2–5 kΩ cm thinned to a thickness of 200 μm. They are fabricated at CiS, Erfurt, Germany. This specific thickness has been chosen because of limitations imposed by the bump-bonding vendor in order to properly perform the Under-Bump Metallisation (UBM). Particular care was taken in the design of the edge termination aiming to minimize dead area without affecting the efficiency of the edge pixels. In the "old" ATLAS three layer Pixel Detector, the sensor design edge consisted in 16 guard rings covering a width of about 600 μm with a safety margin region of 500 μm, adding up to an overall inactive edge of 1100 μm between the edge pixels and the cutting edge. For the IBL design edge the number of guard rings is decreased to 13 and the safety margin width is reduced to ~90 μm. Moreover the edge pixels are extended to 500 μm length so that one half of their surface is placed opposite to the guard rings. With these improvements, the active area defined by the 50% hit efficiency is measured to be approximately 200 μm from the cutting edge [5].

3.1.2. *3D sensors*

The 3D production used 4" FZ p-type high resistivity wafers. These type of wafers, because of their specifications, are normally adopted for fabrication of high resistivity p-type silicon sensors. In the IBL, the 3D-DDTC (Double-sided Double Type Column) technology with 200 μm slim edges has been used. The junction columns are etched from the front side of the wafer and ohmic columns from the back side. The active-edge is not doable, but a fence of ohmic columns was proven to be effective in reducing the dead area at the edges, in order to meet IBL specifications. 3D wafers have been produced by two vendors: CNM-CSIC (Centro Nacional de Microelectronica, Campus Universidad Autonoma de Barcelona, Spain) and FBK (Fondazione Bruno Kessler, Povo di Trento, Italy). At the wafer scale I–V measurements are done to

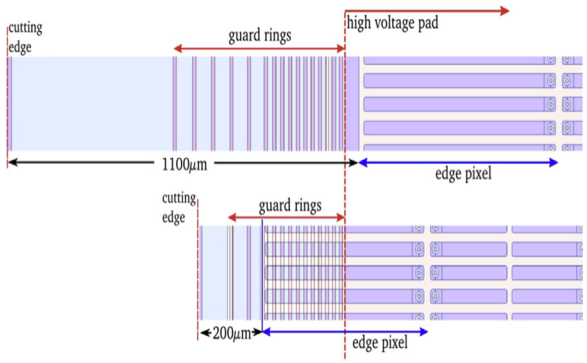

Fig. 2. Comparison of the edge region of the current ATLAS Pixel (APS) design (upper) and the IBL planar sensor design (lower) [5].

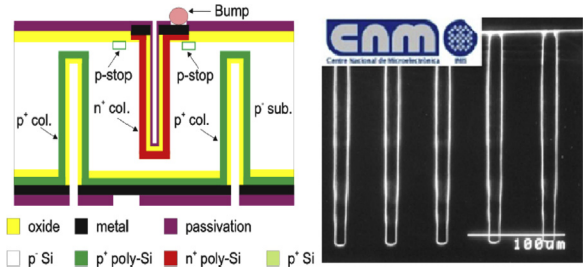

Fig. 3. Sketch and SEM micrographs of 3D etched columns of the CNM pixel sensor design [5].

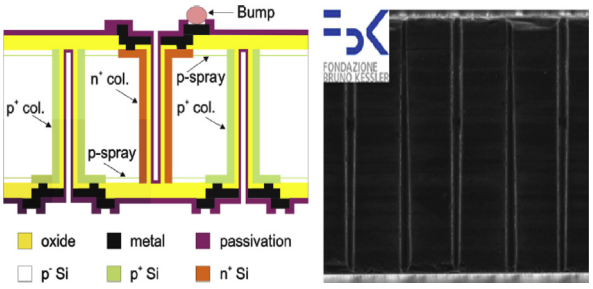

Fig. 4. Sketch and SEM micrographs of 3D etched columns of the FBK pixel sensor design [5].

select good sensor tiles. These are made on each sensor using probe stations. FBK exploits a removable temporary metal allowing a measurement of I–V at the column level while CNM measures the guard ring current only (Fig. 2).

CNM: In CNM sensors the columns do not traverse completely the substrate, but stop at a short distance from the surface of the opposite side. The isolation implantation between the n^+ columns at the surface is made with p-stops on the front size. The slim edge guard ring design is made using the combination of a n^+ 3D guard ring that is grounded and fences that are at the bias voltage from the ohmic side [7] (Fig. 3).

FBK: In FBK sensors the column electrodes traverse the full bulk thickness, requiring p-spray isolation on both sides. The bias- and read-out electrodes are left unfilled after doping [7] (Fig. 4).

3.2. *The FE-I4 read-out chip*

The 3-layer ATLAS pixel detector is built with 16-chip modules using the 7.6×10.8 mm^2 FE-I3 read-out. The FE-I3 has 2880 pixels, with a granularity 400×50 μm^2 in a 250 nm feature size bulk CMOS process. The new FE-I4 chip was designed in 130 nm CMOS technology to cope higher with radiation levels