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Design and TCAD simulation of double-sided pixelated low gain avalanche detectors

Gian-Franco Dalla Betta [a,b,*], Lucio Pancheri [a,b], Maurizio Boscardin [c,b], Giovanni Paternoster [c], Claudio Piemonte [c,b], Nicolo Cartiglia [d], Francesca Cenna [d], Mara Bruzzi [e]

[a] Dipartimento di Ingegneria Industriale, Università di Trento, Via Sommarive 9, 38123 Trento, Italy
[b] TIFPA INFN, Via Sommarive 14, 38123 Trento, Italy
[c] Fondazione Bruno Kessler, Via Sommarive 18, 38123 Trento, Italy
[d] INFN Sezione di Torino, Via P. Giuria 2, 10125 Torino, Italy
[e] Dipartimento di FIsica e Astronomia, Università di Firenze, and INFN Sezione di Firenze, Via Giovanni Sansone 1, 50019 Sesto Fiorentino, Italy

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ABSTRACT

We introduce a double-sided variant of low gain avalanche detector, suitable for pixel arrays without dead-area in between the different read-out elements. TCAD simulations were used to validate the device concept and predict its performance. Different design options and selected simulation results are presented, along with the proposed fabrication process.

1. Introduction

Low Gain Avalanche Detectors (LGADs) are attracting wide interest within the HEP community [1].

These devices are similar to avalanche photodiodes (APDs) normally used for light or X-ray detection [2]. Peculiar to LGADs is that the gain layer doping profile is engineered to yield a low gain (from a few units to a few tens, compared to the relatively higher gain of APDs, that can reach ~1000). In fact, LGADs are mainly intended to detect high energy charged particles, so that their gain should compensate loss of signals due to two possible reasons: the use of thin substrates and charge trapping, that is the most severe phenomenon limiting detector performance at very high irradiation fluencies [3]. To this purpose, gain values of just a few units, like those obtained from heavily irradiated n-on-p sensors biased at very high voltage [4], would be sufficient. On the other hand, in order to boost speed properties for timing applications, gain values in the range from 10 to 30 would be desirable and are here considered as a target [5]. With such low gains, standard read-out circuits could be used without risk of signal saturation; moreover, low gain also ensures low excess noise factor [2].

The first LGAD prototypes developed by CNM Barcelona [1] have been characterized by several groups, showing very promising performance. These devices are potentially able to provide concurrent very good position and timing resolution, a fact that could open new opportunities in particle tracking detectors as well as in other fields. Some studies have highlighted a severe gain reduction in LGADs after irradiation [1,6], so radiation tolerance should be thoroughly addressed in new device developments. In addition, alternative design and fabrication approaches are necessary to pass from pad detectors to strips and pixels. In fact, existing LGADs are built with a single-sided fabrication process, and feature a blank ohmic contact on the back side and read-out junctions on the front side, embedding an additional doping layer to control the avalanche multiplication mechanism and properly designed terminations to prevent from early breakdown at the edge. This works well for pads, but in case of patterned detectors it would lead to large spatial nonuniformities in the signal amplitudes since charge carriers collected at the junction edges would experience reduced (or even null) multiplication. The problem is in fact not new: for fast X-ray imaging applications, arrays of avalanche photodiodes featuring two possible segmentation options (divided cathode and divided anode) have already been proposed, but no details on the detector performance are reported [7].

In this work, we propose a modified, double-sided LGAD structure, having a large multiplication region (n/p junction) on the back side and ohmic read-out pixels on the front side. The device concept has been validated with the aid of TCAD simulations, showing multiplication gains from a few units up to about 30 depending on the

* Corresponding author at: Dipartimento di Ingegneria Industriale, Università di Trento, Via Sommarive 9, 38123 Trento, Italy.
Tel.: +39 0461 283904; fax: +39 0461 281977.
E-mail address: gianfranco.dallabetta@unitn.it (G.-F. Dalla Betta).

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doping concentration of the multiplication layer and on the operational conditions. The design options and selected simulation results will be presented, along with the proposed fabrication process to be implemented at FBK (Trento, Italy).

2. Device description and fabrication strategy

In order to obtain charge multiplication at reasonably low voltages, the avalanche process must be initiated by electrons, that have higher ionization coefficient than holes [2]. Therefore, for highly segmented detectors like pixels, the only feasible option consists in using p^- substrates and fabricating a large, uniform multiplication junction ($n^{++}/p^+/p^-$) on one side, and ohmic pixels (p^{++}/p^-) on the opposite side. Since fast timing circuits might be difficult to embed in small pixels, the multiplication region could also be patterned in macro-pixels (~1 mm^2 area, ~1 pF capacitance) with a small reduction of the geometrical efficiency (~5%). By doing so, different functions could be divided between the two sensor sides, using the pixelated ohmic side for position resolution, and the macro-pixelated junction side for timing resolution [8].

The schematic cross section of the proposed device is shown in Fig. 1. The pixel side at the top is simple, since it just requires one boron implantation or diffusion. On the contrary, the gain side is quite complex, since it requires four different patterned doping layers, to be obtained by a combination of ion implantation and thermal diffusion: the gain layer is made by a thin n^{++} region and an overlapping p^+ region, the latter being the most critical for its impact on the device gain and breakdown voltage. In addition, a proper termination able to prevent edge breakdown is necessary. Taking inspiration from power devices, this can be made of a deep n^+ region equipped with a metal field plate, the so called JTE [9]. Moreover, another patterned p^+ region (p-stop) is used to isolate the n^+ regions [10]. In the proposed device, p-stop is preferred to p-spray in order for its doping profile not to be overlapped to the gain layer.

Not shown in Fig. 1, but essential for the device operation, is a multiple guard-ring termination on the gain side, preventing early breakdown at the periphery [11,12]. To this purpose, existing designs, already tested at FBK and featuring breakdown voltages higher than 1100 V, will be used.

The proposed device has some drawbacks: for pixels made on the ohmic side, isolation requires full depletion and inter pixel resistance after irradiation could be an issue; moreover, it is well known that detectors with hole-reading electrodes are less radiation hard than their electron-reading counterparts. Nevertheless, having timing resolution as the main long-term objective of our project, this approach is deemed appropriate for applications calling for moderate radiation hardness.

Devices will be fabricated at FBK leveraging on the strong experience with Silicon Photo-Multipliers [13]. To control the multiplication properties and the breakdown voltage, the Boron dose of the p^+ gain layer will be used, hence it is the main process parameter considered in the simulations. The first batch of sensors will be fabricated at FBK on relatively thick (275 μm) 6″ wafers, in order to disentangle the issues inherent to LGAD operation from those set by processing thin wafers. However, in order to improve the timing performance, we aim at later work with thinner (~100 μm) substrates. Processing 6″ wafers thinner than 200 μm is not easy and probably not compatible with most of the automatic equipment in the fabrication laboratory. To address this problem, we plan to use thin substrates having a support wafer that should then be selectively removed by local etching based on deep reactive ion etching (normally used for 3D detectors [14]) or chemical etching [15].

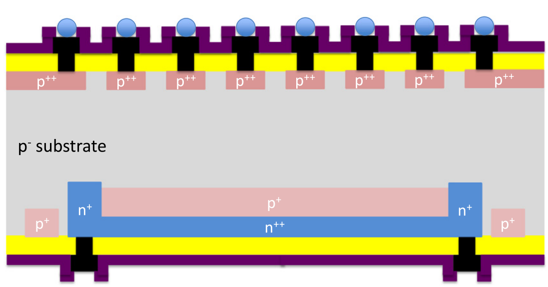

Fig. 1. Schematic cross section of proposed double-sided pixelated low gain avalanche detector (not to scale).

3. TCAD simulations

Simulations have been performed with the Sentaurus Device program, incorporating parameters typical of FBK technology. Depending on the type of simulations, different domains have been used: in particular, 2D simulations were used to predict the electrical characteristics of the devices (e.g., leakage current and breakdown voltage). For the dynamic simulations (charge collection and gain), 2D simulations are not ideal since they do not properly account for the lateral spread of charge clouds, thus overestimating the effects of high charge concentrations [16]. To this purpose, 3D simulations would be the best solution, but they are very time-consuming due to the very large numbers of grid points. Therefore, we have used 2D simulations with cylindrical coordinates that are a good trade-off.

Results are here presented showing direct comparisons between data relevant to the first batch (275 μm thickness) and the future one (100 μm thickness). Fig. 2 shows the breakdown voltage as a function of the boron dose of the gain layer. The dose dependence of the breakdown voltage is pretty high in both cases, and more pronounced in the thicker device, thus confirming the need for fine tuning of this parameter with process splits.

In order to compare the device performance for different thicknesses, we considered two doses providing very similar breakdown voltages of about 1050 V, i.e., 2.6×10^{12} cm^{-2} for 275 μm and 2.1×10^{12} cm^{-2} for 100 μm. Fig. 3 shows the leakage currents as a function of voltage (*I–V*) in the two devices. Simulation results are scaled to pixels of 50 × 50 μm^2 size. Of course, larger current is observed in the thicker device, due to the larger depletion volume. In both cases, impact ionization effects start affecting the leakage current well below the breakdown voltage.

Fig. 4 shows the capacitance curves as a function of voltage (*C–V*), which exhibit a two-phase behavior: at low voltage, the gain layer is initially depleted, then the substrate is depleted until the curves saturate at different values due to the different thicknesses. The transition between the two phases correspond

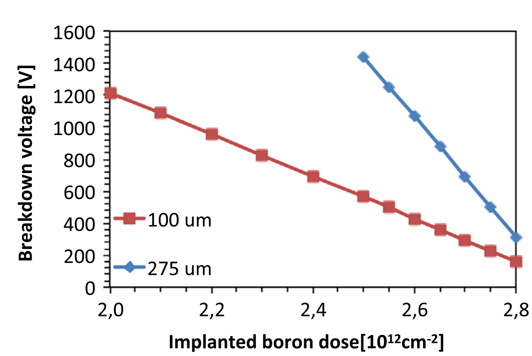

Fig. 2. Breakdown voltage as a function of the boron dose of the gain layer for 100 μm and 275 μm thick sensors.