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Improving charge-collection efficiency of SOI pixel sensors for X-ray astronomy

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ABSTRACT

We have been developing a new type of active pixel sensor, referred to as "XRPIX" for future X-ray astronomy satellites on the basis of silicon-on-insulator CMOS technology. The problem on our previous device, XRPIX1b, was degradation of the charge-collection efficiency (CCE) at pixel borders. In order to investigate the non-uniformity of the CCE within a pixel, we measured sub-pixel response with X-ray beams whose diameters are 10 μmΦ at SPring-8. We found that the X-ray detection efficiency and CCE degrade in the sensor region under the pixel circuitry placed outside the buried p-wells (BPW). A 2D simulation of the electric fields with the semiconductor device simulator HyDeLEOS shows that the isolated pixel circuitry outside the BPW makes local minimums in the electric potentials at the interface between the sensor and buried oxide layers, where a part of charge is trapped and is not collected to the BPW. Based on this result, we modified the placement of the in-pixel circuitry in the next device, XRPIX2b, for the electric fields to be converged toward the BPW, and confirmed that the CCE at pixel borders is successfully improved.

1. Introduction

X-ray charge-coupled devices (CCDs) are standard imaging spectrometers widely used in X-ray astronomy because of their fine pixel pitch (~20 μm) and good energy resolution (~130 eV in FWHM at 6 keV) [1–3]. However, CCDs suffer from problems such as poor time resolution (a few seconds) and a high non-X-ray background especially above 10 keV due to high energy particles in orbit. Thus, we have been developing active pixel sensors, referred to "XRPIX", for future X-ray astronomy satellites, which allow us to achieve observation with a high-speed readout and a low background.

XRPIX is fabricated using a silicon-on-insulator (SOI) CMOS technology [4] and consists of the following three layers: a low resistivity Si layer for circuits with a thickness of ~8 μm, a high resistivity depleted Si layer for X-ray detection with a thickness up to 500 μm, and a buried oxide (BOX) layer with a thickness of ~0.2 μm for insulation between the two layers (Fig. 1). Each pixel has a sense node of p+ in the sensor layer connected with the circuit through a via in the BOX layer. A buried p-well (BPW) is implemented around the sense node to suppress the back-gate effect on the circuit and also collects signal charge and transfer it to the sense node because BPWs are implanted so high as to be ohmic [4]. The pixel readout circuit has a trigger capability with time resolution better than 10 μs [5]. The in-pixel trigger circuit also enables event-driven readout, with which we can achieve a low non-X-ray background by using an anti-coincidence technique with surrounding scintillators.

Matsumura et al. [6] found the degradation of the charge-collection efficiency (CCE) at the pixel borders of our second device, XRPIX1b [7,8]. In this paper, we report on the results of the X-ray beam experiment of XRPIX1b and of investigation using our improved device, XRPIX2b. We discuss the causes of the degradation based on the results and determine its solution.

2. Experiment with 10 μmΦ X-ray beams

2.1. Experimental setup

We performed measurement of sub-pixel response of XRPIX1b by irradiating with parallel X-ray beams whose diameters are

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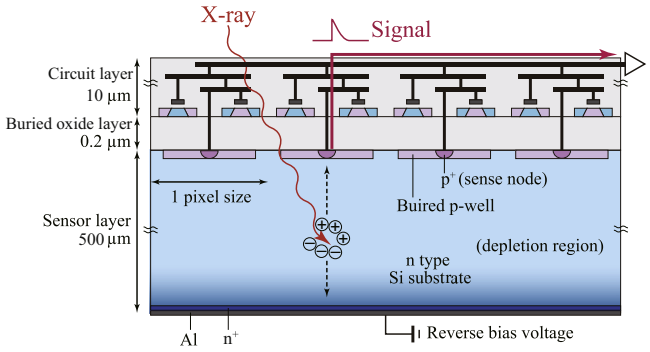

Fig. 1. Schematic cross-sectional view of XRPIX.

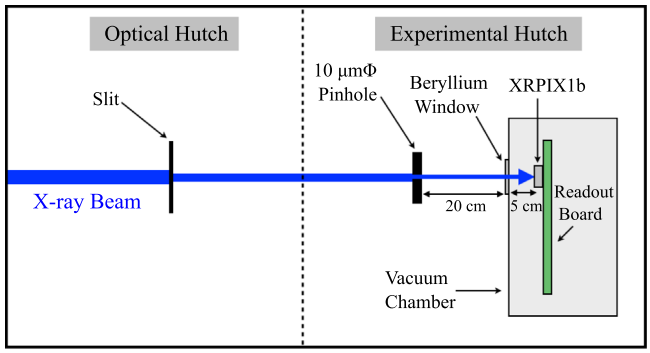

Fig. 2. Schematic of the experimental setup.

10 μmΦ at BL29XUL of SPring-8 [9]. XRPIX1b has a pixel size of 30.6 μm × 30.6 μm, a format of 32 × 32 pixels, and a depletion thickness of 500 μm.

Fig. 2 shows the schematic of the experimental setup, which was previously used for the measurement of a point-spread function of CCD devices [10]. The X-ray beam is shaped with a slit in the optical hutch and a 10 μmΦ pinhole placed in front of a beryllium window attached to the vacuum chamber where XRPIX1b and its readout board are installed. The beam intensity on the sensor place is uniform inside a diameter of 10 μm, because the beam size before collimation is sufficiently larger than 10 μm. The distances from the pinhole and the device to the beryllium window are 20 cm and ≤ 5 cm, respectively. X-rays illuminate the front-side of the device. We cooled the device to about -50 °C in order to reduce dark current using a pulse tube cooler attached to a copper cold plate. The vacuum pressure was lower than $\sim 10^{-4}$ Pa throughout experiment. We scanned with a 6 μm step size and recorded the data at each step. The measurement was performed twice, one with an 8.0 keV beam and the other with a 17.7 keV beam. The irradiated pixels are identical between the 8.0 keV and 17.7 keV measurement.

We applied a bias voltage of 200 V with which the sensor layer is fully depleted (~ 500 μm). In the measurement, we performed frame-by-frame readout in which all the pixels are sequentially read out after a 1 ms exposure. The details of the readout sequence are presented in Ryu et al. [7].

2.2. Result of the SPring-8 beam experiment

We show the X-ray counts maps obtained from the 8.0 keV and 17.7 keV measurement in Fig. 3 in which the count rates are normalized with the maximum counts in each map. We corrected X-ray counts for 35% and 10% beam-intensity drifts observed during the 8.0 keV and 17.7 keV measurement, respectively. The count rates drop periodically at the pixel size in both the 8.0 keV and 17.7 keV cases and the pattern is similar to each other. Thus, it is very natural to assume that the positions at the minimum and maximum count rates in the two maps correspond to the identical locations in the device, although the precise positions of the pixel centers in the maps are unknown a priori. Accordingly, (a) and (d) in Fig. 3 with the maximum count rates, (c) and (f) with the minimum count rates, and furthermore (b) and (e) have identical positions in the device. In the map for 8.0 keV, the detection efficiency relative to (a) is (79 ± 3)% and (22 ± 3)% at (b) and (c), respectively. In the map for 17.7 keV, the detection efficiency relative to (d) is (97 ± 3)% and (81 ± 3)% at (e) and (f), respectively. These results suggest that there are 70–100 μm thick dead regions at (c)/(f) in the sensor layer near the interface with the BOX layer because attenuation lengths of 8.0 keV and 17.7 keV X-rays are 60 μm and 640 μm in silicon, respectively.

Fig. 4 shows the spectra of 8.0 keV X-rays. While signal charge of a single-pixel event is generated in the central region of a pixel, charge is generated at the pixel border split into two adjacent pixels and results in a double-pixel event. In the spectra obtained at (a), we see a single line (red solid) as expected. However, in the spectra at (b), the peak energies of double-pixel events are significantly lower than those of single-pixel events, and the spectra at (c) have no line. Thus, the CCE degrades at (b) and (c) where the dead regions are.

2.3. Comparison of pixel circuits and count rates map

Matsumura et al. [6] suggested that the distortion of electric fields in the sensor layer degrades the CCE [6]. The shape of the electric fields at the interface region between the BOX and sensor layers is determined mainly by electric potentials of the structures existing there, i.e. the sense node, the BPW, and in-pixel circuitry (see Fig. 1). Therefore, we compare the in-pixel circuit layout and the count rates map of 8.0 keV X-rays in Fig. 5. We did a by-eye fit so that the sense node and the BPW correspond to the areas with high detection efficiency. As a result, we found that the CCE and detection efficiency are generally low at the pixel borders as suggested by Matsumura et al. [6].

3. Simulation of electric fields and potentials in XRPIX1b

According to Fig. 5, it seems in general that the detection efficiency outside the BPWs is low in the regions where the circuitry is located, suggesting that the existence of circuitry affects the detection efficiency and the CCE outside the BPWs. In order to confirm it, we ran a 2D simulation of the electric fields and potentials along the cross-section connecting two sense nodes given in Fig. 6(i). We used the semiconductor device simulator HyDeLEOS, which is a part of the TCAD system HyENEXSS [11]. We fixed the electric potentials of the sense nodes and the BPWs at 0 V, and the back bias at 200 V. The voltages of the pixel circuits located 0.2 μm above the BOX are variable between 0 V and 1.8 V, and so we ran two simulations with the pixel circuit voltages fixed at 0 V and 1.8 V. We found no difference between the two cases. It is well known that fixed charge is generated in the BOX layer during the wafer process. We assumed a typical fixed charge of $2.0 \times 10^{11}\,\mathrm{cm}^{-2}$ taken from the literature [12,13]. We simulated with the charge uniformly distributed between 1 nm and 3 nm above the sensor-BOX interface.

Fig. 6(ii) shows that the electric fields under C–D penetrate into the region where the circuitry exists while those under A–B and E–F converge into the BPWs. The electric potentials in the sensor layer close to the interface with the BOX layer are presented in Fig. 6(iii). The signal charge under A–B or E–F is transported to the BPWs and is detected by the sense node without any significant loss. On the other hand, the charge under C–D is carried to the