Nuclear Instruments and Methods in Physics Research A 787 (2015) 340–343

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

Electrical characterization and simulation of SiPMs

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ARTICLE INFO

Available online 28 January 2015

Keywords:
SiPM
Single photon detection
Equivalent circuit
Impedance measurement

ABSTRACT

Silicon Photomultipliers (SiPMs) are versatile and sensitive photon detectors that experience a fast growing variety of use in particle physics and related fields of application. These photo detectors have a very promising photon detection efficiency and are therefore interesting for very low light flux applications such as scintillation and fluorescence light detection. As a semiconductor device the SiPM's gain and time response strongly depend on the operating temperature and voltage. Thus they have to be understood for a proper use of the SiPM. Therefore, accurate electrical simulations of the SiPM's behavior involving electrical readout and front-end electronics help to improve the design of experimental setups, since several different designs can be tested and simulated with a manageable amount of effort. To perform these simulations, a detailed equivalent circuit of the SiPM has to be used containing a set of well-defined parameters.

For this purpose, SPICE simulations of SiPMs and readout electronics have been performed. These simulations utilize an improved SiPM model consisting of resistors, capacitances and inductances. The SiPM parameters for these simulations have been determined by measuring the impedance over a wide frequency range while applying a DC voltage in forward direction and various DC voltages from zero up to the SiPM breakdown voltage in order to determine the behavior under operating conditions. The impedance measurements, the electrical model and the resulting simulations are presented. The impact of different setups and the electrical properties of the SiPM is discussed.

1. Introduction

Silicon Photomultipliers (SiPMs) are tiny and compact semiconductor devices for light detection at single-photon level.

These devices have a growing field of use in particle and medical physics. Because of their semiconductor nature, SiPMs are very sensitive to temperature variations and their applied bias voltage. An electrical equivalent circuit has been introduced including the voltage dependency of the pn-junction. Impedance measurements have been performed to determine the circuit's parameters. These measurements have been done with different instruments to cover a huge frequency range. Using these measurements, SPICE simulations can be performed to investigate the signal output of different electronic designs for front-end electronics. This allows for an assessment of the electrical performance of amplifiers and power supply with less prototyping.

2. Electrical equivalent circuit

The equivalent electrical circuit is shown in Fig. 1. The circuit consists of SiPM cells and additionally parasitic components that are used for the whole SiPM.

Every SiPM cell consists of a diode capacitance (C_D) that represents the p–n-junction within the SiPM as it is assumed as a parallel plate capacitor. The diode capacitance is discharged during a cell breakdown. A quenching resistor (R_Q) is placed in series to the diode capacitance as it is done in the real SiPM. Every real resistor has a parasitic capacitance that is called quenching capacitance (C_Q). These three devices form a SiPM cell.

To simulate parasitic effects of the routing grid and connection pins on the SiPM a grid capacitance (C_G) is introduced. This electrical equivalent circuit is based on work of Corsi et al. [1]. Related publications are [2–4].

In addition to this model a bulk inductance (L_B) and a bulk resistance (R_B) are used. These devices help to model the impedance behavior at high frequencies (see Section 3). Furthermore, the bulk inductance is the only device within the circuit that limits the slope of the rising edge in the SiPM output signal.

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http://dx.doi.org/10.1016/j.nima.2015.01.066
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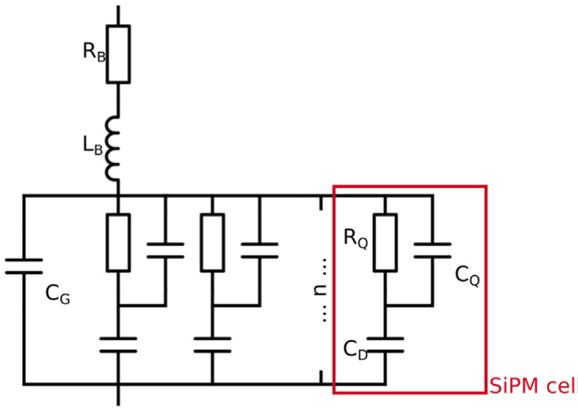

Fig. 1. Electrical equivalent circuit of a SiPM.

The absolute impedance depending on the measurement frequency can be calculated using this model and yields

$$|Z(\omega)| = \left| i\omega L_B + R_B + \left(i\omega C_G + n \left(\frac{1}{i\omega C_D} + \frac{1}{R_Q^{-1} + i\omega C_Q} \right)^{-1} \right)^{-1} \right|. \quad (1)$$

3. Measurements of electrical parameters

The values of the electrical parameters of the SiPM's equivalent circuit can be determined by measuring the impedance over a wide frequency range and fitting formula (1) to the measured data. These measurements were taken with an Agilent E4980A LCR meter in the frequency range from 20 Hz to 2 MHz and an Agilent E5061B-3LF LF-RF network analyzer in the frequency range from 100 kHz to 500 MHz. A DC voltage of up to 40 V can be applied when using the LCR meter. The measurement voltage amplitude is kept on a low level (50 mV) to reduce a variation of the p–n-junction depth during the measurement.

In a first step, the quenching resistance is measured. During this measurement a DC voltage of 2 V is applied to the SiPM in forward direction. The measurement frequency is set to 20 Hz. Thus, the diode capacitance of the p–n-junction vanishes. The quenching capacitance and the grid capacitance have very high impedances due to the low frequency and do hardly contribute to the total impedance. The inductance has a very low impedance due to the measurement frequency. The (ohmic) impedance is then calculated by

$$R_Q = \frac{|Z_{measured}|}{n} \quad (2)$$

with the measured impedance value $Z_{measured}$ and the number of SiPM cells n.

In a next step, the impedance is measured without applied bias voltage over the whole frequency range. The remaining electrical parameters are determined by a fit to this measurement. A typical impedance curve including the fit is shown in Fig. 2. In the last step, the impedance curve is measured for applied bias voltages up to 40 V with the LCR meter. A new fit is done while all parameters but the diode capacitance are kept constant. Thus the diode capacitance can be measured up to 40 V (see Fig. 3). To determine the diode capacitance at the SiPM's operating voltage of ~70 V the diode capacitance is extrapolated using

$$C_D(U_{bias}) \propto U_{bias}^{-1} \quad (3)$$

as the expected behavior of a parallel plate capacitor [5]. Using this procedure yields the values for an S10362-33-050C Hamamatsu MPPC shown in Table 1.

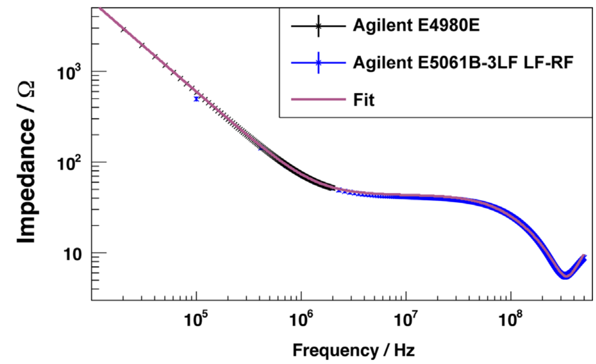

Fig. 2. Impedance measurement and applied fit for an S10362-33-050C Hamamatsu SiPM with 3600 cells at zero bias voltage in the frequency range from 20 Hz to 500 MHz

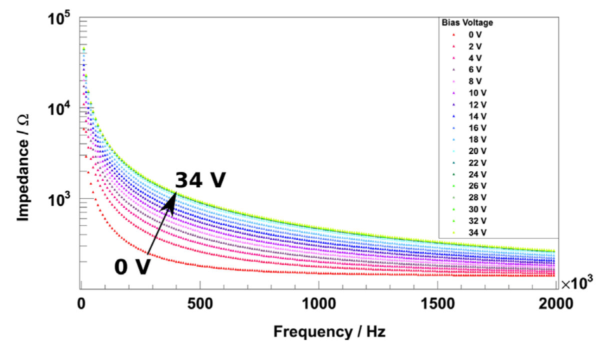

Fig. 3. Impedance measurement of an S10362-33-100C Hamamatsu MPPC with 400 cells at bias voltages from 0 V to 34 V in the frequency range from 20 Hz to 500 MHz

Table 1
Electrical parameters for an S10362-33-050C Hamamatsu MPPC obtained with impedance measurements. The uncertainties are the statistical uncertainty obtained by the fit.

Parameter	Value	Uncertainty	Unit
R_Q	143.7	0.2	k Ω
C_D	774.1	0.3	fF
C_Q	6.2	0.2	fF
C_G	27.4	0.8	pF
L_B	4.71	0.02	nH
R_B	3.27	0.03	Ω

4. A new measurement adapter for bias voltages up to 100 V

Standard commercial devices for the measurement of impedance do not allow for a connection mechanism for SiPMs and the possibility to connect an external bias voltage source simultaneously. For this reason a custom version of a measurement adapter has been designed that is capable of these functions. This adapter should be useable with the GWInstek LCR-8110G meter since this device is going to be used for further measurements instead of the Agilent LCR meter. The LCR-8110G has a frequency range from 20 Hz to 10 MHz. The main challenge is to design a device that can decouple voltages of up to 100 V and has very low parasitic characteristics. The decoupling of the bias voltage from the measurement device is done with ceramic capacitors with a capacity of 10 μF. A few diodes are used to reduce the risk of high voltages applied to the LCR meter. A circuit diagram is shown in Fig. 4.

Three different printed circuit boards were produced according to the diagram. To characterize them an open-circuit measurement and a closed-circuit measurement were conducted. These measurements were then compared to the same measurement