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An analog cell to detect single event transients in voltage references ☆

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ABSTRACT

A reliable voltage reference is mandatory in mixed-signal systems. However, this family of components can undergo very long single event transients when operating in radiation environments such as space and nuclear facilities due to the impact of heavy ions. The purpose of the present paper is to demonstrate how a simple cell can be used to detect these transients. The cell was implemented with typical COTS components and its behavior was verified by SPICE simulations and in a laser facility. Different applications of the cell are explored as well.

1. Introduction

Some electronic systems are designed to work in harsh environments, such as avionics, space, nuclear facilities or linear accelerators [1,2]. In these environments, energetic heavy ions hit the electronic devices generating a high density of free carriers. If this happens in internal capacitances, such as gate oxides or reverse-biased PN junctions, the cloud is swept away by the electric field and an instantaneous current transient occurs, which is transmitted into the system.

With the exception of some mixed-signal components [3,4], the only expected soft errors in analog devices are single event transients (SETs) due to the absence of memory elements. In particular, some works have reported that voltage references can show a very dangerous kind of SET called "long duration pulse" (LDP) [5,6]. In special circumstances, the transients last for several hundreds of μs or even 1 ms. This characteristic is critical in analog-to-digital (A/D) or digital-to-analog (D/A) conversions [7]. In general, the output of a D/A or A/D converter is proportional to either V_{REF} or V_{REF}^{-1}. If a peak Δv_{REF} appears, it is easy to demonstrate that the analog or digital output shows a percentage error of $\pm \Delta v_{REF}/V_{REF}$. Voltage references are usually built using a core cell (e.g., band-gap cells or Zener diodes) followed by an operational amplifier (op amp) (Fig. 1). The core cell provides a reference value (V_{CORE}) independent of the power supply or the temperature whereas the op amp stabilizes the system by negative feedback, scales the reference voltage, and improves the output characteristics. Usually, voltage references must provide current to the load. Thus, a simple class-A output stage is an efficient and widely used solution (Q_O and I_Q in Fig. 1) [5].

LDPs in voltage references are a dangerous hazard since they lead to hundreds or thousands of erroneous conversions [5,8]. In this paper, we are going to demonstrate how a very simple analog cell able to detect SETs beyond a tunable threshold value can help to solve this undesirable issue.

2. The cell and its properties

The proposed cell is shown in Fig. 2. In this cell, only passive components and two comparators are required. The input of the cell is *REF* and two warning digital signals (Rising Pulse Warning, *RPW*, and Falling Pulse Warning, *FPW*) are the outputs. Let us calculate the bias point, *Q*, accepting that the comparators have a high input impedance. It follows then that:

$$V_{A,Q} = \frac{R_2 + R_X}{R_T} \cdot V_{REF,Q} \tag{1}$$

$$V_{B,Q} = \frac{R_2}{R_T} \cdot V_{REF,Q} \tag{2}$$

R_T being $R_1 + R_2 + R_X$. At the bias point, $V_A = V_{AF} = V_{AR}$ and $V_B = V_{BF} = V_{BR}$ so $\Delta V_{BA} = -R_X/R_T \cdot V_{REF,Q} < 0$. Therefore, the outputs of both comparators are in the LOW state. Now, let us suppose that a

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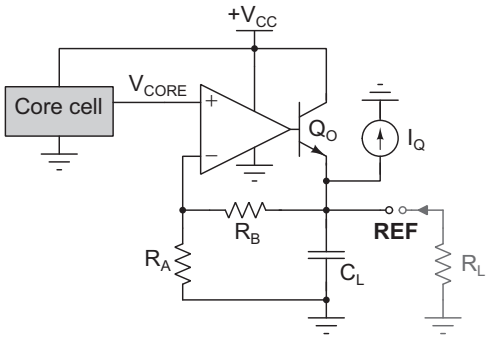

Fig. 1. Standard voltage reference. A core cell, biased by the power supply, $+V_{CC}$, provides a stable voltage value (V_{CORE}) that works as the input of a non-inverting amplifier. Thus, $V_{REF}=(1+(R_B/R_A))\cdot V_{CORE}$. Typically, the output is just a class-A stage consisting of an NPN (or NMOS) transistor, Q_O, and a current source, I_Q, to bias it in the forward-active zone. The capacitor is included to filter noise. R_L represents a hypothetical load.

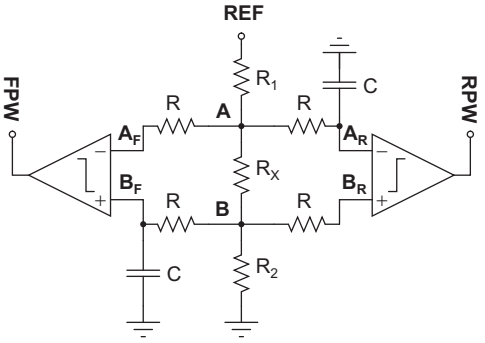

Fig. 2. Proposed surveying cell. The output signals are the Rising Pulse Warning, *RPW*, and the Falling Pulse Warning, *FPW*. Some resistors are included to minimize the effects of the input bias currents. In comparators with open collector/drain output, additional pull-up resistors (R_{PU}) and a logic power supply ($+V_L$) are necessary.

transient occurs at *REF*. This transient can be modeled as a perturbation, $\pm v_{PK}$, around the bias point. Thus, during the transient, $V^*_{REF}=V_{REF,Q}\pm v_{PK}$. The following step is to set the time constant, $\tau=R\cdot C$, much longer (e.g., one order of magnitude) than the worst-case transient duration. Given that the transient duration is $\sim$10–1000 μs [5,6,9], τ must be selected on the order of 0.1–10 ms. In this situation, the perturbation quickly reaches nodes A and B as well as nodes A_F and B_R, which are open circuits in practice. However, nodes A_R and B_F are not immediately affected due to the presence of the capacitors. Therefore, ΔV_{BA} becomes positive in one of the two comparators and its output switches to HIGH indicating the occurrence of an SET. Namely, rising transients, with $v_{PK}>0$ trigger *RPW*, whereas *FPW* is activated by falling transients.

Now, the cell will be analyzed in a quantitative way. Instead of resolving the circuit in the frequency domain, we are going to use the standard technique in the field of small-signal circuits research, which consists in modeling the capacitors as short-circuits in AC mode. Later, DC and AC contributions will be added using the superposition principle.

Hence, it can be demonstrated that one of the comparators is triggered if v_{PK} falls outside the interval $[-V_{THF},V_{THR}]$ with:

$$V_{THR}\approx\frac{R_X}{R_2}\cdot V_{REF,Q} \tag{3}$$

$$V_{THF}\approx\frac{R_X}{R_2+R_X}\cdot V_{REF,Q} \tag{4}$$

if $R\gg R_1,R_2$. Also, if $R=R_1=R_2$:

$$V_{THR}\approx\frac{2R_X}{R}\left(1+\frac{1}{2}\frac{R_X}{R}\right)\cdot V_{REF,Q} \tag{5}$$

$$V_{THF}\approx\frac{2R_X}{R}\left(1-\frac{3}{2}\frac{R_X}{R}\right)\cdot V_{REF,Q} \tag{6}$$

Anyhow, if $R_X\ll R_2$, $V_{THR}\approx V_{THF}$. An interesting feature is that, as the thresholds are defined as percentage values, the cell functions whatever the reference voltage. Finally, the analysis remains valid once the network has reached the bias point. Therefore, the cell does not work immediately after powering-up the system, the delay being on the order of τ.

It is interesting to check how non-idealities compromise the performance of the cell. First of all, let us investigate the effects of the resistor tolerance. For the sake of brevity, only the situation in which $R\gg R_1,R_2$ will be described. According to the error propagation theory, the uncertainty of V_{THR}, ΔV_{THR}, is related to the resistor tolerance as

$$\frac{\Delta V_{THR}}{V_{THR}}=\frac{\Delta R_X}{R_X}+\frac{\Delta R_2}{R_2} \tag{7}$$

as it is easily deduced from Eq. (3). Therefore, precision resistors are strongly recommended.

Another interesting parameter to take into account is the input offset voltage of the comparators. For example, if $R\gg R_1,R_2$, the rising transients are detected if:

$$v_{PK}>V_{THR}+\frac{R_T}{R_2}\cdot V_{OS,R} \tag{8}$$

and the falling ones if:

$$|v_{PK}|>V_{THF}+\frac{R_T}{R_2+R_X}\cdot V_{OS,F} \tag{9}$$

$V_{OS,R}$ and $V_{OS,F}$ being the input offset voltages of the comparators that detect **R**ising and **F**alling transients. Another parameter that can affect the performance of the cell is the input bias current of the comparators. In Fig. 2, we can see that every input of the comparators is connected to the nodes AF, AR, BF and BR. This will be the guideline to denominate the corresponding input bias currents. Defining them positive if flowing into the device, calculations show that they contribute to the effective input offset voltage as

$$\Delta V^*_{OS,R}=\frac{R_X}{R_T}[R_2\cdot(I_{BF}+I_{BR})-R_1\cdot(I_{AF}+I_{AR})]-R\cdot(I_{BR}-I_{AR}) \tag{10}$$

$$\Delta V^*_{OS,F}=\frac{R_X}{R_T}[R_2\cdot(I_{BF}+I_{BR})-R_1\cdot(I_{AF}+I_{AR})]-R\cdot(I_{BF}-I_{AF}) \tag{11}$$

The influence of the input bias currents is minimized if currents are extremely low or, if $R_1=R_2$, identical to cancel each other out.

3. Simulations in SPICE

In order to verify the functioning of the analog cell we carried out simulations using realistic SPICE models of commercial-off-the-shelf (COTS) discrete components found in the literature on electronic systems for space. The voltage reference was created using an LM124A SPICE micromodel in non-inverting configuration, which is an improved version of the one that was successfully used by the authors to investigate SETs in networks with op amps [6,10,11].

Concerning the output stage, the NPN transistor was modeled as a typical 2N2222A. Furthermore, the current source, I_Q, was removed since the feedback resistor network, R_A and R_B, managed to correctly bias the transistor in forward-active zone. Other parameters of the simulated voltage reference were $V_{CORE}=1.25$ V, $R_A=33$ kΩ, $R_B=100$ kΩ, which yield $V_{REF}=5.0$ V.