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FPGA-based klystron linearization implementations in scope of ILC

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ABSTRACT

We report the development and implementation of four FPGA-based predistortion-type klystron linearization algorithms. Klystron linearization is essential for the realization of ILC, since it is required to operate the klystrons 7% in power below their saturation. The work presented was performed in international collaborations at the Fermi National Accelerator Laboratory (FNAL), USA and the Deutsches Elektronen Synchrotron (DESY), Germany. With the newly developed algorithms, the generation of correction factors on the FPGA was improved compared to past algorithms, avoiding quantization and decreasing memory requirements. At FNAL, three algorithms were tested at the Advanced Superconducting Test Accelerator (ASTA), demonstrating a successful implementation for one algorithm and a proof of principle for two algorithms. The functionality of the algorithm implemented at DESY was demonstrated successfully in a simulation.

Besides this, a proof of principle of an FPGA-based klystron and cavity simulator implemented at the High Energy Accelerator Research Organization (KEK), Japan, was demonstrated. Its purpose is to allow the development and test of digital LLRF control systems including klystron linearization algorithms when no actual klystron and cavity are available.

1. Introduction

Klystrons are widely used for the high level radio frequency (HLRF) generation for driving cavities in particle accelerators. It is planned to adapt this technology at the International Linear Collider (ILC) [1,2]. At ILC the klystrons will be one element in the chain of the digital low level RF (LLRF) control loop. Typically the input to output characteristics of a klystron in both amplitude and phase are not linear. A schematic of a typical input-to-output amplitude characteristic is shown in Fig. 1 (black). In order to perform field regulation, typically klystrons are operated about 40% below saturation. In order to operate the klystrons at ILC most cost effectively, it is intended to operate them 7% (in power) below the point of saturation. At this point the slope of the input-power-to-output-power characteristics is only about $\frac{1}{10}$ compared to the slope at the linear region. Since the control gain is proportional to this slope, it also degrades close to the point of saturation. In order to keep the feedback effective, it is required to keep the slope of the input-to-output amplitude characteristic constant. Furthermore it is preferable to introduce an output amplitude limiter and to eliminate any output phase rotation. The desired klystron output characteristics in amplitude and phase are shown in Fig. 1 (red dashed lines) in the respective plots. Such output characteristics can be accomplished by using a klystron linearization. The linearization algorithms described in the following are predistortion-type linearizations, implemented in the firmware of the Field Programmable Gate Array (FPGA), on which besides others the controller is located. The predistortion added is the inverse of the non-linear characteristics of the klystron. It is typically generated in dependency of the signal amplitude and applied after the controller and the addition of feedforward tables and before transmission to the Digital-to-Analog Converters (DACs).

Linearization concepts were already implemented in the past using analog circuits. Over the recent years improved capabilities of FPGAs allowed not only the implementation of digital LLRF feedback controllers but also the implementation of klystron linearization algorithms with high effectiveness and flexibility. Four algorithms implemented on FPGAs of two different manufacturers are described and compared in the following.

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2. Klystron linearization implemented at DESY

At DESY the Free Electron Laser in Hamburg (FLASH) [3] is operated, which uses the same superconducting TESLA-type 9-cell cavity technology [4] as will be used in ILC. The digital LLRF control system at FLASH was based on the VME standard, before it was updated to MTCA.4 [5]. For the VME system a predistortion-type squared amplitude dependent direct lookup table (LUT)-based klystron linearization was implemented [6,7], which allowed a complex correction corresponding to

$$\begin{pmatrix} I' \\ Q' \end{pmatrix} = \begin{pmatrix} f_i(A^2) & -f_q(A^2) \\ f_q(A^2) & f_i(A^2) \end{pmatrix} \begin{pmatrix} I \\ Q \end{pmatrix} \quad (1)$$

where I and Q are the input of the linearization algorithm, $f_i(A^2)$ and $f_q(A^2)$ are the correction factors, and I' and Q' are the output of the algorithm.

Since the FPGAs assembled on the VME controller card and on the MTCA.4 controller card are different, the formerly programmed algorithm could not be reused. Thus, as a part of the presented study, the algorithm was reintroduced for the MTCA.4-based LLRF control system [8]. The schematic of the implemented VHDL package is shown in Fig. 2.

From the I and Q input signals the squared amplitude is computed using two multipliers and one adder. The resulting word is truncated to the appropriate bit length and used as the address of the lookup tables. The output words of both lookup tables are applied to input I and Q values corresponding to a complex multiplication using four multipliers, one adder, and one subtracter. The resulting signals are truncated to signals with the appropriate bit lengths called I' and Q' and are outputted.

One unique feature of the implementation presented is the compatibility with the FPGAs on the MTCA.4-based hardware used at DESY. This means the klystron linearization package can be implemented and used not only in the digital LLRF control system at FLASH but also at the upcoming European X-Ray Free Electron Laser (European X-FEL) [9]. A second unique feature of the presented package is an improved MATLAB script for the generation of the lookup tables, which delivers more accurate results, especially at low input amplitudes.

3. Klystron linearization implemented at FNAL

At FNAL ASTA [10] is under construction. Since it is beside an user machine also an ILC R&D accelerator, the digital LLRF control system was designed with ILC in mind.

As part of the presented study, three kinds of predistortion-type amplitude dependent klystron linearization algorithms were implemented and tested. The target hardware was the FPGA on the multi-cavity field control (MFC) module [11]. The first algorithm implemented was designed for the linearization of the amplitude only [8]. Its principle is based on the following equation:

$$\begin{pmatrix} I_{out} \\ Q_{out} \end{pmatrix} = f_{corr}(A) \begin{pmatrix} I_{in} \\ Q_{in} \end{pmatrix} \quad (2)$$

Fig. 3 shows a schematic of the linearization algorithm implemented. From the I_{in} and Q_{in} input values, the amplitude A is computed by $A = \sqrt{I_{in}^2 + Q_{in}^2}$. For the implementation of the square root function, a proprietary block of the Altera DSP Builder library was used. By a 3rd-order-polynomial-function depending on the amplitude A, a correction factor f_{corr} is calculated. Furthermore, an amplitude limitation is included, which compares the expected output amplitude to a preset limit. If the limit is exceeded, the correction factor is set to $f_{corr} = limit/A$. If the limit is not exceeded, the correction factor is not changed and applied to the I_{in} and Q_{in} input values. By two switches the linearized or the original I_{in} and Q_{in} values can be chosen as the output I_{out} and Q_{out}, respectively.

The second implemented linearization algorithm was an upgrade of the previous one. With the upgrade the support of phase

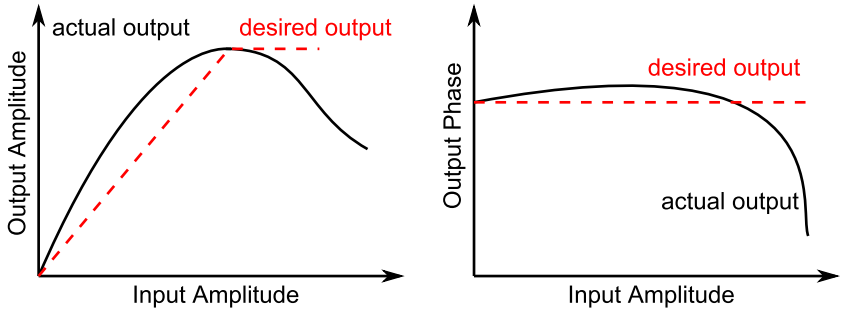

Fig. 1. Schematic of the klystron amplitude and phase output characteristics. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

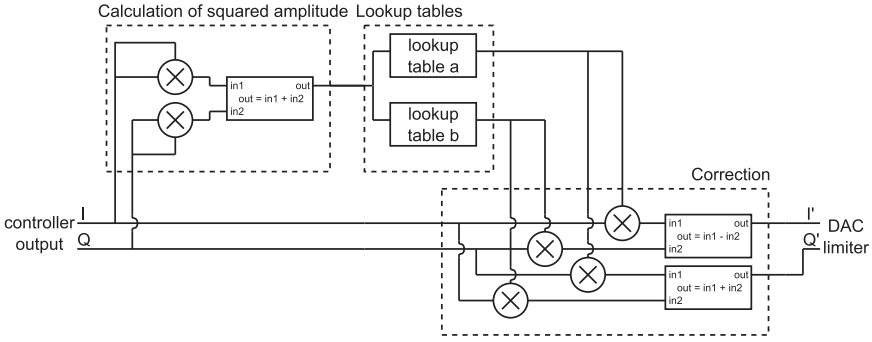

Fig. 2. Schematic of the direct lookup table-based klystron linearization package.