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Development of novel on-chip, customer-design spiral biasing adaptor on for Si drift detectors and detector arrays for X-ray and nuclear physics experiments

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ABSTRACT

A novel on-chip, customer-design spiral biasing adaptor (SBA) has been developed. A single SBA is used for biasing a Si drift detector (SDD) and SDD array. The use of an SBA reduces the biasing current. This paper shows the calculation of the geometry of an SBA and an SDD to get the best drift field in the SDD and SDD array. Prototype SBAs have been fabricated to verify the concept. Electrical measurements on these SBAs are in agreement with the expectations. The new SDD array with an SBA can be used for X-ray detection and in nuclear physics experiments.

1. Introduction

Si spiral drift detector (SSDD) [1–3] is a special type of Si drift detector (SDD) family [4] that utilizes a cylindrical geometry and ion implants as both the rectifying junction and voltage divider. A voltage divider is needed to create a potential gradient (or drift field) in an SDD for carriers generated by incident particles to drift to the collection anode, as shown in Fig. 1. A near-cylindrical, or square geometry has been used in this work as it is the best unit cell to make an uniform array in two dimension space. The optimum surface potential profile $\Phi(r)$ on the front surface that gives a minimum drift time of electrons had been calculated using the calculus in Ref. [1] for an uniform backside bias voltage of V^B, and in Ref. [5] for a double-sided spiral SDD as shown in Fig. 1.

The advantage of using a spiral as a voltage divider is that one can easily calculate the design with non-constant pitch ($p(r)$) and width ($W(r)$) and fabricate it, which gives a largely exotic surface potential distribution that guaranties a minimum carrier drift time. To do the same with an external resistor chain, one would have to choose resistors varying from hundreds of kilo ohms to mega ohms of values that are not commercially available.

In general, the double-sided spiral SDD, as shown in Fig. 1, can also be used for better surface field distributions needed for obtaining a minimum drift time of carriers [5]. Here, the start of the spiral is at $r=r_1$, and the end is at $r=R$. However, since the rectifying junction and voltage divider are coupled together in the conventional spiral SDD, there is a constraint of the ratio of spiral width to pitch ($W(r)/p(r)$) for more uniform drift field in the drift channel. This results in a large spiral current I_S for a given voltage difference ($V_{out}-V_{E1}$) between the start (V_{E1} at $r=r_1$) and end (V_{out} at $r=R$). Heat generated by the spiral stays inside the SDD, which may cause problem to cool down the detector. More importantly, for a spiral SDD array of substantial number of cells, the power consumption (P) can be relative big: $P=N\times(V_{out}-V_{E1})\times I_S$, where N is the number of array cells, approaching many watts for $N>100$.

For a single spiral SDD, its power consumption is about 2.5 mW, which is not too big to handle. But since the heat generated by the spiral heats up the SDD itself, it aggravates the cooling problem. This is due to the fact that in order to achieve low noise, we need to cool the detector to a fixed low temperature value to reach a low enough leakage current. More heat source in the detector will make this cooling more difficult.

Furthermore, for a SDD array of at least 10×10 cells, in addition to the heating problem, the power consumption can be too large as well, close to watts.

To solve these problems while retaining the advantage of the implant spiral as a voltage divider, we propose a SDD array system

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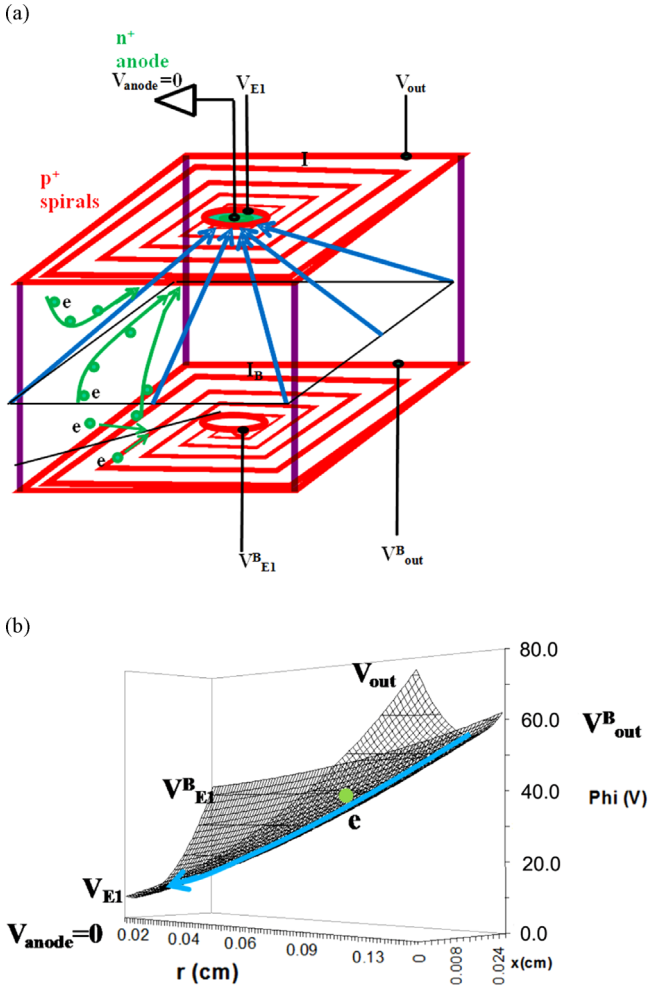

Fig. 1. (a) Illustration of a double-sided spiral SDD, and (b) the corresponding negative potential profile.

that utilizes an implant chip of spiral biasing adapter (SBA), and an SDD array with closed concentric rings that are interconnected.

2. The concept of spiral biasing adapter (SBA)

As shown in Fig. 2, for a conventional spiral SDD (square type) with a side length of $L=3$ mm (or a drift radius of $R=1.5$ mm), the width $W(r)$ was fixed to be 2/3 of the pitch $p(r)$ to assure a more uniform electric field in the bulk. For a constant drift field in the drift channel (which gives a carrier minimum drift time), the ohmic current running through the spiral that defines the front surface potential profile has to be about 20 μA at a bias of 126 V for the detector we are studying. The spiral current is determined to be large enough to avoid the affection of the voltage distribution by the SDD leakage current. If we would like the SDD leakage current to be smaller than 1% of the current of the SBA, then one SBA can be used to bias up to 25 cm^2 (for a leakage current of about 10 nA/cm^2). We consider here an array of 10×10 concentric SDD cells of 5×5 mm and apply a safety margin. Since the use of an SBA reduces the heat as compared to the spiral SDD, it may improve the SDD spectroscopic resolution for one can cool an SDD down to a lower temperature (smaller leakage current). Applying an SBA has little effect on the dimension of anode. As compared to the standard external biasing apparatus, the effect of SBA on the reduction of system noise is minimal, but using an SBA can reduce carrier drift time.

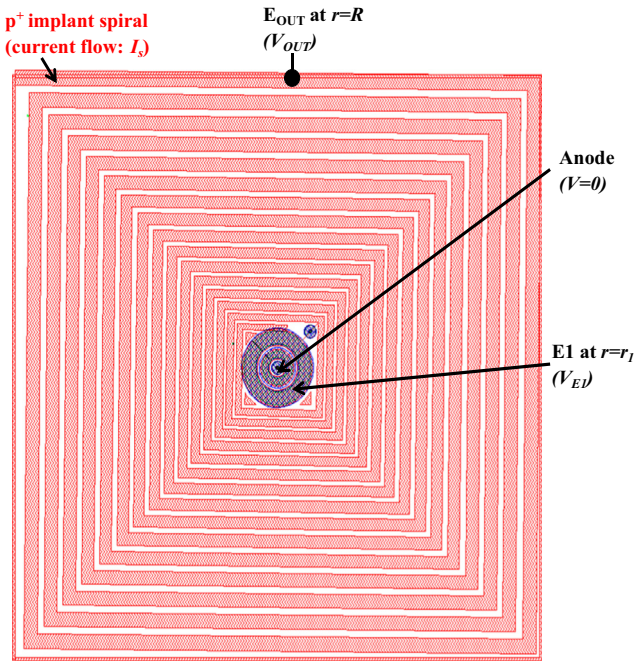

Fig. 2. An example of customer-design spiral of p^+-implant, which provides minimum drift time for electrons with a given set of bias voltages and spiral current.

The pitch of an SBA ($p_{BSA}(r)$) and its implant width ($W_{BSA}(r)$) have been chosen to get a minimum carrier drift time for a given set of biasing voltages and the spiral current, as shown in Fig. 3a). The rectifying junctions in a single SDD cell are defined by concentric rings (not spirals). The pitch of a single SDD cell in the array is the same as that of the SBA ($p_{SDD}(r))=p_{BSA}(r)$), as shown in Fig. 3b), but its width can be defined with freedom. In general the trace widths of SDD is made bigger, i.e. $W_{SDD}(r)) \geq W_{BSA}(r)$, to minimize the surface area on the SDD. A good design rule can be $W_{SDD}(r))=\eta\cdot p_{SDD}(r)$, with $\eta\geq0.7$. In our design, we make $\eta=0.8$ (Fig. 3b).

3. Interconnections between SBA chip and SDD chip, and between SDD cells

An SBA is designed and fabricated on the same wafer as the SDD while its ion implant is the same as that of the SDD array, which makes the SBA a simple and convenient by-product of the SDD array fabrication. The best arrangement of an SBA and the SDD array is to detach the SBA and SDD array (dicing apart the SBA and SDD array), and interconnect each winding of the SBA with the corresponding ring in one single SDD cell in the array by wire bonding, as shown in Fig. 4. This is a more desirable arrangement since (1) usually there are not more than 30 rings of SDD (or windings in SBA), so the number of wire bonding is not too big; (2) since the dimension of a single SDD (L) is usually <5 mm, so the wire bond length is also $<L$, which is doable; and (3) an SBA is physically separated from the SDD array, so there is no heat generated in the SDD array at all.

A second option is to use the double-metal technology to interconnect an SBA and the SDD array. While this method will be simple and easier, it could provide a heat source and as a consequence a temperature gradient to the SDD array. The most convenient interconnections between single SDD cells in the array can be done by double-metal technology, as shown in Fig. 5. However, for small array and small single SDD dimension (small number of rings), interconnecting the SDD chips with wire bonds