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Radiation-hard/high-speed parallel optical links

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ABSTRACT

We have designed an ASIC for use in a parallel optical engine for a new layer of the ATLAS pixel detector in the initial phase of the LHC luminosity upgrade. The ASIC is a 12-channel VCSEL (Vertical Cavity Surface Emitting Laser) array driver capable of operating up to 5 Gb/s per channel. The ASIC is designed using a 130 nm CMOS process to enhance the radiation-hardness. A scheme for redundancy has also been implemented to allow bypassing of a broken VCSEL. The ASIC also contains a power-on reset circuit that sets the ASIC to a default configuration with no signal steering. In addition, the bias and modulation currents of the individual channels are programmable. The performance of the first prototype ASIC up to 5 Gb/s is satisfactory. Furthermore, we are able to program the bias and modulation currents and to bypass a broken VCSEL channel. We are currently upgrading our design to allow operation at 10 Gb/s per channel yielding an aggregated bandwidth of 120 Gb/s. Some preliminary results of the design will be presented.

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1. Introduction

A parallel optical engine allows a compact design for high-speed data transmission. The design is enabled by readily available high-speed VCSEL arrays. With the use of a 12-channel array operating at 10 Gb/s per channel, a parallel optical engine can deliver an aggregate bandwidth of 120 Gb/s. With a standard spacing of 250 μm between VCSELs, the width of a 12-channel array is only slightly over 3 mm. This allows the fabrication of a rather compact parallel optical engine for installation in locations where space is at a premium. Besides the reduced physical size, there are other advantages in using an array solution. For example, one can reserve 1 in 12 channels for redundancy instead of doubling the number of channels if using a single-channel VCSEL. This is therefore a much more efficient scheme to implement redundancy by bypassing a dead channel. The array scheme also reduces the service requirements by using one power supply to bias each array instead of a single power supply for each VCSEL channel. Additionally, the use of a fiber ribbon reduces the number of fibers to handle and moreover a fiber ribbon is less fragile than a single-channel fiber. These multiple advantages greatly simplify the production, testing, and installation of optical links.

VCSEL arrays are widely used in off-detector data transmission in high-energy physics. The first implementation of VCSEL arrays for on-detector application is in the optical links of the ATLAS pixel detector. The experience from the operation has been quite positive. In particular, the failure rate of the optical links fabricated by The Ohio State University is $\sim 0.1\%$. Modern VCSELs are humidity tolerant and hence no special precautions are needed. The ATLAS experiment plans to continue the use of VCSEL arrays in a new layer of the pixel detector, the insertable barrel layer (IBL), to be installed in the initial phase of the LHC luminosity upgrade.

In response, we have designed an ASIC for possible use in the IBL project. The ASIC is a 12-channel VCSEL array driver capable of operating up to 5 Gb/s per channel. We will present some measurements of the characteristics of the ASIC below. We have also modified the design for operation at 10 Gb/s per channel and some preliminary design will be presented.

2. Results from a 5 Gb/s VCSEL array driver

The VCSEL array driver ASIC is designed to operate at a speed up to 5 Gb/s. The planned operating speed for the IBL optical link is 160 Mb/s but we designed the ASIC to operate at much higher speed to gain experience in the design of a high-speed array driver. The ASIC was fabricated in a 130 nm CMOS process to enhance the radiation-hardness [1]. The radiation-hardness by design techniques employed in the chip, including the use of

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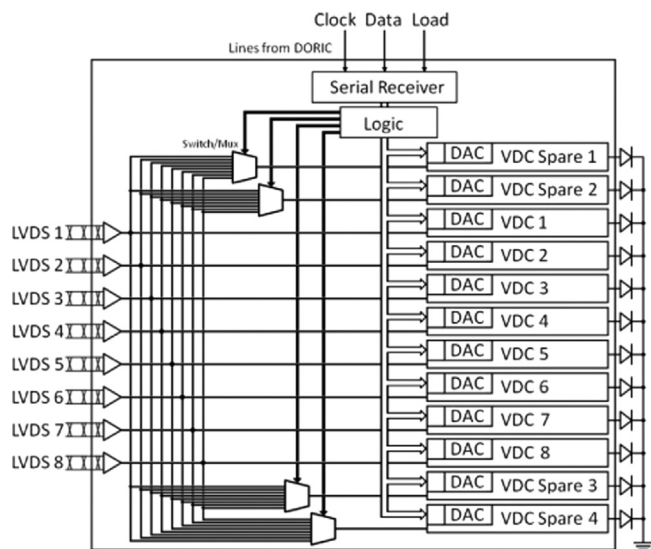


Fig. 1. A 12-channel VCSEL array driver ASIC.

enclosed layout transistors when the thick oxide variant of the processes transistors were used, were based on test results and guidelines provided by the CERN microelectronics group [2,3]. The ASIC is an improved version of the driver designed with a 250 nm CMOS process for use in the optical links [4] of the installed pixel detector of the ATLAS experiment. Several improvements were incorporated into the new ASIC taking advantage of experience gained from building and operating the first array-based optical links and will be detailed below.

Each ASIC contains eight low voltage differential signal (LVDS) receivers to receive the data from the front-end electronics. A block diagram of the ASIC is shown in Fig. 1. The received LVDS signal is converted in the driver stage into a current sufficient to drive a VCSEL. The amplitude of the modulation current in each driver is controlled via an 8-bit DAC. There is also a single 8-bit DAC to set the bias currents of all of the channels simultaneously. In addition, there are four spare drivers with associated 8-bit DACs that can receive the LVDS signal from any of the eight LVDS receivers via a switching network. This allows the received LVDS signal to be transmitted via one of the four spare VCSEL channels should a VCSEL in one of inner eight channels become non-operational. To enable operation in case of a failure in the communication link to the receiver array ASIC, we have included a power on reset circuit that will set the modulation current in the VCSEL to 9 mA on top of a bias current of 1 mA upon power up with no signal steering.

The 8-bit DAC and LVDS receiver are designed to operate with a 1.5 V supply and the driver stage is designed to operate with a 2.5 V power supply. A higher supply voltage is required by the output stage to allow enough headroom to drive VCSELs which normally have threshold voltages of 2 V or higher.

We have characterized several ASICs. Each ASIC is coupled to a VCSEL array fabricated by ULM with a bandwidth of 10 Gb/s [5]. The current consumption for the 2.5 V supply is measured to 250 mA with all channels active at 5 Gb/s. The power consumption for the 1.5 V supply is 30 mA. The ASIC can supply at least 10 mA of drive current to a VCSEL, producing an optical power in excess of 1 mW coupled into a fiber.

The optical eye diagram of a channel in the driver ASIC is shown in Fig. 2. It is evident that the eye diagram readily satisfies the IEEE specification with a clear separation between the signal traces and the mask [6]. We simulated the ASIC using the extracted layout to investigate the cause of the bi-modal jitter in the eye diagram. The simulations indicate that the bi-modal jitter originated in the LVDS

receiver which then propagated through the rest of the circuit. Thus, we will focus further efforts on improving the design of the LVDS receiver.

This eye diagram is for the case in which only one VCSEL driver channel is active. Fig. 3 shows the eye diagram with all channels active, a more realistic operating condition. It should be noted that all channels in the ASIC were driven with the same pseudo-random input signal but delays introduced by cabling and buffer chips distributing the signals effectively desynchronize the signals into each VCSEL driver channel. It is evident that the jitter is somewhat larger but that the eye diagram still satisfies the IEEE specification. With all channels active at 5 Gb/s, we detect no bit errors in 33 min of operation. This corresponds to a bit error rate (BER) of $< 2.3 \times 10^{-13}$ at 90% confidence level. The random jitter of the ASIC is measured to be $R_j = 3$ ps and deterministic jitter to be $D_j = 37$ ps. This can be used to estimate a total jitter using the following equation:

$$T_j = D_j + \alpha(\text{BER}) \times R_j$$

For the target BER of 10^{-12} [7], $\alpha = 14.07$. This yields a total jitter of 72 ps.

As noted above, the ASIC also contains several added functionalities to make the optical links more reliable and easier to operate, motivated by the experience in operating the first on-detector optical links based on VCSEL arrays. This includes a power-on reset circuit that sets the ASIC to a default configuration with no signal steering in case of a failure in the communication link to the ASIC. This feature has been successfully implemented. We also verified that the bias and modulation currents of the individual channels are programmable.

The redundancy circuit is an important feature implemented for the bypassing of a broken VCSEL. The integrity of the steered signal in the spare channel has been tested by steering the signal through the maximum distance from a channel on one side of the ASIC to the spare channel on the other side. Fig. 4 shows the optical eye diagram of this signal. The steered signal has more jitter as expected but the eye diagram still satisfies the IEEE specification.

3. Preliminary design of a 10 Gb/s VCSEL array driver

We are currently designing a 10 Gb/s VCSEL driver to yield an aggregated bandwidth of 120 Gb/s when coupled to a 12-channel VCSEL array. A central question of the design is what semiconductor process to use. We expect both 130 nm SiGe BiCMOS and 65 nm CMOS to have the sufficient bandwidth. However, due to cost consideration, we will first attempt to design the driver using the 130 nm CMOS process to see if this is practical.

The 5 Gb/s VCSEL driver uses thick oxide transistors in order to provide sufficient voltage to drive the VCSEL. This is not practical for the high-speed operation due to the increased parasitic capacitance/inductance. We therefore modify the architecture to use thin oxide transistors and add a negative VCSEL bias voltage in addition to the +1.5 V supply voltage.

We have a preliminary design for the driver stage of the ASIC. The design has been laid out. We have simulated the extracted layout with parasitic capacitance, inductance, and resistance from the VCSEL itself and the wire bonds and pads used for connecting the VCSEL to the ASIC. The parasitics used for the ASIC and bond pads are provided by our ASIC design extraction software. For the bonds themselves we use a lumped model provided in [8]. The custom VCSEL model used includes a diode with parameters adjusted to match the IV characteristics of the VCSEL under test and a capacitance provided by the vendor. The simulated eye diagram of the driver stage is shown in Fig. 5. It is evident that the eye diagram is open. However, we are working to center the eye

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