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Development of $N+$ in P pixel sensors for a high-luminosity large hadron collider

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ABSTRACT

Hamamatsu Photonics K. K. is developing an $N+$ in a p planar pixel sensor with high radiation tolerance for the high-luminosity large hadron collider (HL-LHC). The $N+$ in the p planar pixel sensor is a candidate for the HL-LHC and offers the advantages of high radiation tolerance at a reasonable price compared with the $N+$ in an n planar sensor, the three-dimensional sensor, and the diamond sensor. However, the $N+$ in the p planar pixel sensor still presents some problems that need to be solved, such as its slim edge and the danger of sparks between the sensor and readout integrated circuit. We are now attempting to solve these problems with wafer-level processes, which is important for mass production. To date, we have obtained a 250-μm edge with an applied bias voltage of 1000 V. To protect against high-voltage sparks from the edge, we suggest some possible designs for the $N+$ edge.

1. Introduction

Several candidates exist to serve as pixel sensors for the high-luminosity large hadron collider (HL-LHC), such as the $N+$ in a p planar sensor, the $N+$ in an n planar sensor, the three-dimensional (3D) sensor, and the diamond sensor. Hamamatsu Photonics K. K. has been developing an $N+$ in the p planar pixel sensor with high radiation tolerance for the HL-LHC.

The $N+$ in the p planar sensor offers several advantages, the first of which is its cost effectiveness. Because $N+$ in p planar sensors is fabricated by a simple wafer process with masks only on a single side, the process has good yield compared with other types of sensors. In addition, in the high radiation environment, the lifetime of the $N+$ in p planar sensor is longer than that of other $P+$ in n sensors fabricated via the single-side process [1]. Because the $N+$ in the p sensor does not rely on induced type inversion after irradiation, it is possible to read signals even when the sensor is partially depleted (i.e., after the full depletion voltage has exceeded the bias voltage applied after irradiation).

However, $N+$ in p planar sensor type also has certain disadvantages, the first of which involves the width of the inactive edge, which is typically wider than the $N+$ in the n planar sensor [2] and the 3D sensor [3]. The second problem involves sparking between the sensor and the readout application-specific integrated circuit (ROIC), which occurs because the edge of $N+$ in the p sensor is exposed to high voltage and the gap between sensor and ROIC is only 20 μm. If we can overcome these problems, the $N+$ in the p planar sensor would be very competitive. Herein, we report preliminary results of research that aims to resolve these problems.

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2. Slim edge

2.1. Previous results

Pixel sensors are located at the heart of large complex detectors and serve to track signals close to the interaction point. This area contains a lot of important signals, so detecting all tracks is desirable. However, it is not realistically possible to detect all tracks that cross a pixel sensor because of the dead area of sensors. The edge of an ordinary pixel sensor constitutes such a dead area because a certain distance is needed to prevent the depletion region from contacting the dicing edge.

In a previous study [4], by shrinking the distance from the active area to the dicing edge to 400 μm, we obtained a tolerance of over 1000 V (see Figs. 1 and 2). However, at 1000 V and with less than 400 μm from active area to dicing edge, the depletion region contacted the dicing edge, and a significant leakage current flowed from the dicing edge. Thus, 1000 V tolerance was not possible with an edge distance of less than 400 μm.

2.2. Slim edge process

To overcome this limit, a new technology had to be developed to prevent the depletion region from contacting the sensor edge.

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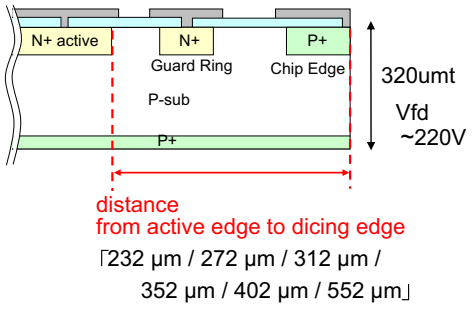

Fig. 1. Cross-section of previous slim-edge trial. The edge was shrunk by a simple planar process.

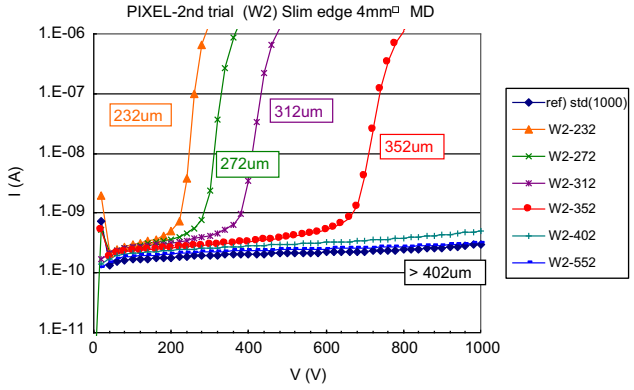

Fig. 2. *I–V* curves from previous slim-edge trial. For an edge distance of less than 400 μm, the voltage tolerance was less than 1000 V.

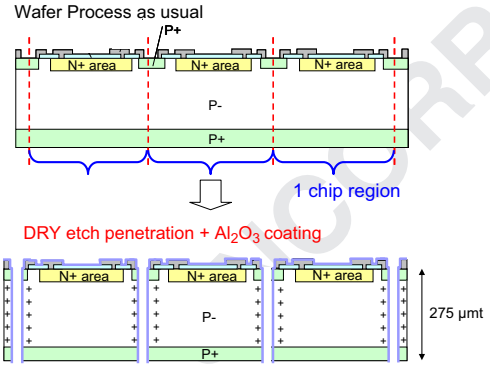

Fig. 3. Process flow for slim-edge trial.

We based our approach on the sidewall Al_2O_3 passivation trial by SCIPP [5] and expanded the technology to the wafer process. Note that completing the process on wafer form is important for mass production.

For our first trial, we used a square 4-mm monitor diode and made one side the slim edge. Fig. 3 shows the process flow.

1. Fabricate *PN* junction and metallize as usual.
2. Penetrate through wafer by dry etching. In this trial, standard trench width was 200 μm, and in addition, we confirmed 20 μm width trench also went well.
3. Deposit Al_2O_3 by atomic layer deposition (ALD). Just before the deposition, we executed a process of eliminating a thin native oxide layer. The total thickness of Al_2O_3 was 30 nm. Al_2O_3 layer made by ALD gives good coverage of the side wall. The Si–Al_2O_3 or SiO_2–Al_2O_3 interface makes positive charges at the Si surface. The depletion layer and negative space charge in the *p*-type wafer are suppressed by the positive charges that accumulate at the Si surface, and the depletion region does not touch the sensor edge. Thus, no leakage current flows from the sensor edge.
4. The final process is dicing of non-slim edge lines.

2.3. Test pattern to evaluate minimum distance

To evaluate the minimum distance, we fabricated a test pattern consisting of a 4-mm monitor diode with a single slim-edge side, as shown in Figs. 4 and 5. We made four types, which were distinguished by the distance from the active area to edge of 210, 250, 290, and 310 μm.

The current–voltage (*I–V*) results are shown in Fig. 6. The data indicating a tolerance of 1000 V is obtained for over 250 μm from the active area to slim edge. In addition, we also confirmed the poor *I–V* characteristics and low voltage tolerance when Al_2O_3 passivation was not used. Thus, the Al_2O_3 charge effect contributed to the good *I–V* characteristics, which implies that the depletion region was not contacting the sensor edge.

For the 210-μm edge pattern, breakdown occurred at 700 V. However, by observing the hot electrons [6], we confirmed that the breakdown occurred between guard-ring *N*+ and edge *P*+. This breakdown was induced by the strong electric field across the narrow *PN* gap, not by contact between the slim edge and depletion region. Thus, by optimizing the design, we may obtain a tolerance of 1000 V with an edge of less than 200 μm. This work is planned for the near future.

2.3. Apply slim edge to a 20-mm pixel sensor for FE-I4 ATLAS-upgrade

As mentioned in the previous section, we confirmed the 250-μm slim edge by using a 4-mm monitor diode. Next, we applied this technology to a real pixel sensor for the FE-I4 ATLAS upgrade. The pixel sensor surface area is about 20×20 mm^2 and the thickness is 275 μm. We fabricated slim edges on three sides by Si penetration and Al_2O_3 passivation.

As shown in Fig. 7, slim-edge distances in this trial were 310 and 480 μm, which are wider than those for the trial described in

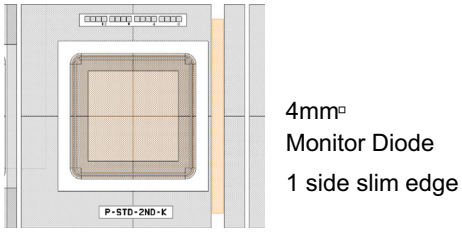

Fig. 4. Top view of test pattern consisting of 4-mm monitor diode and a single slim-edge side. Q5

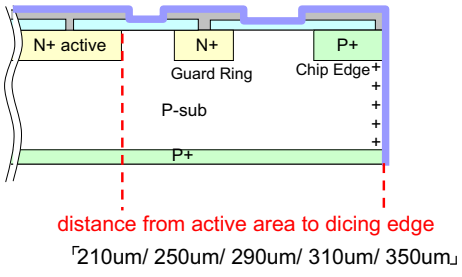

Fig. 5. Cross-section of test pattern.