Nuclear Instruments and Methods in Physics Research A 765 (2014) 209–213

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

Readout chip for the CMS pixel detector upgrade

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ARTICLE INFO

Available online 11 June 2014

Keywords:
CMS
Pixel detector
Upgrade
Readout chip
ROC

ABSTRACT

For the CMS experiment a new pixel detector is planned for installation during the extended shutdown in winter 2016/2017. Among the changes of the detector modified front end electronics will be used for higher efficiency at peak luminosity of the LHC and faster readout. The first prototype versions of the new readout chip have been designed and produced. The results of qualification and calibration for the new chip are presented in this paper.

1. Introduction

For the CMS experiment [1] at CERN an upgrade of the pixel detector is foreseen. The new detector will be adapted to the projected luminosity of 2×10^{34} cm^{-2} s^{-1} that LHC will deliver after machine upgrades which is a factor of 2 above the original design value [2].

1.1. The present pixel detector

The present detector [3] is designed to provide three hits for tracking. This is achieved by three barrel layers and two endcaps on each side (see Fig. 1) that cover a pseudorapidity range of $|\eta| < 2.2$. Almost hermetic enclosure of the interaction point is achieved through overlapping detector design. The three barrel layers are located just outside the beam pipe at $r = 4.4$, 7.3, and 10.2 cm and are made of 768 modules with approximately 48 million channels in total. High η coverage is accomplished by two endcap discs at $z = \pm 32.5$ and ± 46.5 cm. The number of channels for the full detector is 66 million with a power consumption of approximately 3.6 kW. Sensors are segmented into pixels of 100 μm in $r\phi$ and 150 μm in z (for the barrel) and the detector achieves an impact parameter resolution of 28 μm (transverse) and 45 μm (longitudinal) for tracks with transverse momentum $p_T > 10$ GeV/c [4].

The detector is designed for operation at an instantaneous luminosity up to 10^{34} cm^{-2} s^{-1} and for this range it has excellent performance. More than 95% of channels are still operative and the hit efficiency at 4×10^{33} cm^{-2} s^{-1} is greater than 99.0% [2].

1.2. The upgrade pixel detector

The main motivation for the pixel detector upgrade [2] is maintaining the high efficiency when the LHC surpasses its design luminosity of 10^{34} cm^{-2} s^{-1} by a factor of two. The upgrade design provides four pixel hits to improve tracking in the large track multiplicity per collision event that results from the increased luminosity. The fourth hit is provided by an additional barrel layer at $r = 16$ cm as well as an additional endcap disc on each side (see Fig. 2). The design of the endcap discs changes in the upgrade to adopt module types that are very similar to the barrel modules which facilitates production. The new endcaps will be inserted at $z = 29.1$ cm, 39.6 cm, and 51.6 cm.

In order to improve vertex resolution the innermost pixel layer will be moved closer to the interaction point. This requires the exchange of the beam pipe with another of smaller diameter. The innermost pixel layer will then have a radius of 2.95 cm while the other barrel layers will remain at approximately the same radii: $r = 6.8$ cm and 10.9 cm.

The increase to four pixel hits in the upgrade and the thereby needed increase in number of channels must be accommodated with the existing signal fibers. To meet all these requirements the front-end electronics of the detector need to be upgraded.

An improvement of the support structure with light materials and the change from a liquid cooling system with C_6F_{14} [5] to 2-phase CO_2 cooling with much smaller and more lightweight pipes will maintain the material budget despite the increased number of layers. By moving cable connector boards out of the tracking volume the material budget of the upgrade in higher η ranges will be smaller compared to the current detector.

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http://dx.doi.org/10.1016/j.nima.2014.06.011
0168-9002/

1.3. The current readout chip

Modules of the current detector in the barrel are made of 16 readout chips (ROC) that are bump-bonded to one silicon sensor. They are wirebonded to a high density interconnect (HDI) on top of the module (see Fig. 3).

The ROCs consist of 4160 pixels that are grouped into 26 independently operating double columns. Pixels have a programmable charge threshold above which they are sensitive to hits. Upon receiving a hit pixels record the pulse height for readout. Hit information has to be stored during the trigger latency of 3.9 μs. Each double column reads the hits into two buffers for this purpose: The timestamp buffer with a depth of 12 cells and a data buffer that holds the pulse height and pixel addresses with a depth of 32 cells. Pixel hits which are not trigger validated are discarded. The readout of trigger verified hits is coordinated through a token that passes between ROCs.

In some situations inefficiencies related to the ROC design can occur: During the time a trigger validated double column is waiting for the token to initiate readout it does not register further hits. Another mechanism of inefficiency is the limited speed of the column drain that is used to collect the address and pulse height information from the pixels. Data losses also occur if the timestamp buffer or the data buffer overflow or with the reset after each readout of the double column. For the luminosity range the detector is designed for these inefficiencies amount to only a few percent, however higher luminosities will cause substantial losses, mainly due to timestamp and data buffer limitations.

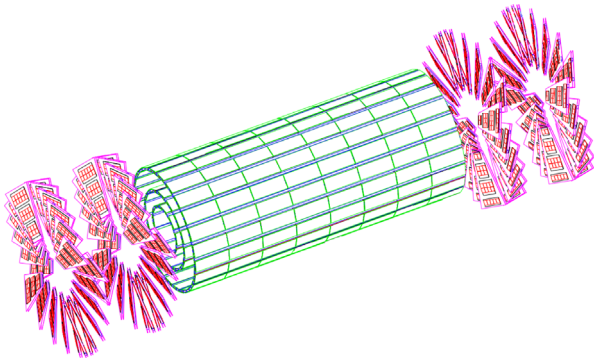

Fig. 1. The geometry of the current pixel detector with three barrel layers and two endcap discs.

1.4. Motivation for the ROC upgrade

With the changed geometry of the upgraded detector and the increased luminosity of the LHC the pixel hit rate will be as much as 4–5 times higher than the rate the current ROC was designed for. The higher rate together with the increased number of channels has to be read out through existing data fibers. In order to meet this requirement the readout speed has to be increased. Additionally, when changing the chip design an opportunity for improving the lifetime of the detector layers exists. This can be achieved by lowering the pixel charge comparator threshold which allows the detector to be operated with lower charge yield caused by sensor irradiation Fig. 4.

2. Changes in the ROC design

2.1. Maintaining efficiency at high rates

A large fraction of the inefficiency at high rates is due to overflows of the internal buffers which are required to store data

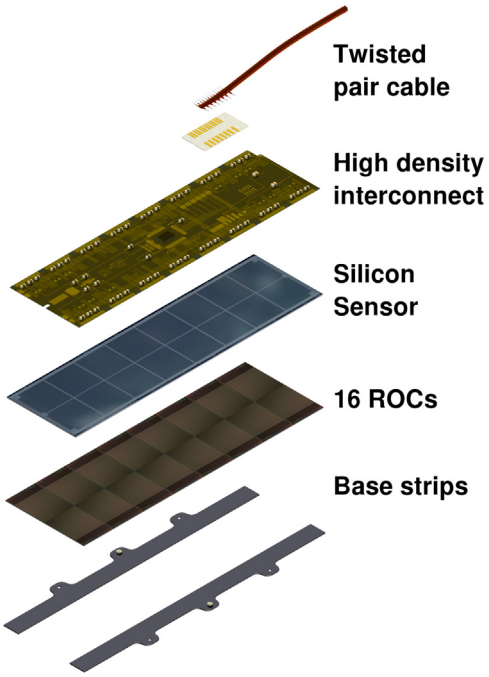

Fig. 3. The components of an upgrade barrel pixel module for layer 2–4.

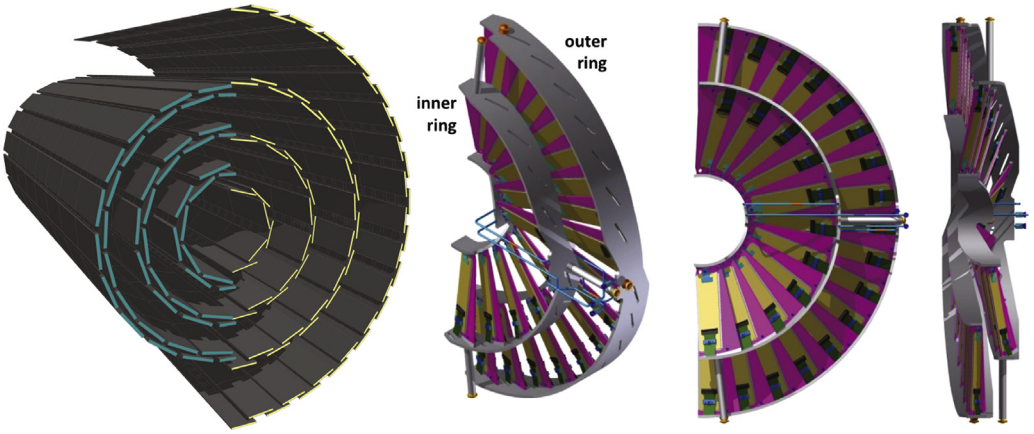

Fig. 2. The pixel detector geometry for the upgrade with four barrel layers and three endcap discs. The image on the left shows the comparison between the current and the upgrade barrel, the other images show the new layout of the endcap discs [2].