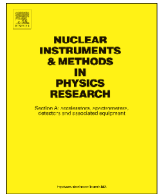




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Low-resistance strip sensors for beam-loss event protection

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ABSTRACT

AC-coupled silicon strip sensors can be damaged in case of a beam loss due to the possibility of a large charge accumulation in the bulk, developing very high voltages across the coupling capacitors which can destroy them. Punch-through structures are currently used to avoid this problem helping to evacuate the accumulated charge as large voltages are developing. Nevertheless, previous experiments, performed with laser pulses, have shown that these structures can become ineffective in relatively long strips. The large value of the implant resistance can effectively isolate the “far” end of the strip from the punch-through structure leading to large voltages. We present here our developments to fabricate low-resistance strip sensors to avoid this problem. The deposition of a conducting material in contact with the implants drastically reduces the strip resistance, assuring the effectiveness of the punch-through structures. First devices have been fabricated with this new technology. Initial results with laser tests show the expected reduction in peak voltages on the low resistivity implants. Other aspects of the sensor performance, including the signal formation, are not affected by the new technology.

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1. Introduction and proposal

One of the operational concerns for silicon strip trackers is the scenario of a beam loss. The past experience shows that sensors can get damaged in this case. The AC-coupled sensors can develop very large voltages across the coupling capacitor. The metal read-out traces are held close to ground due to the low input impedance of the readout amplifier (~ 1 k Ω), while the strip implants could reach a significant voltage in the case of large charge accumulation in the bulk [1], which can occur in the instance of beam loss. In extreme cases the electric field can collapse causing the implants and backplane of the sensor to float to large voltages damaging the capacitors, which are typically qualified to 100 V breakdown voltages.

In order to prevent these large voltages, the punch-through (reach-through) effect is commonly used [2], where strips develop low impedance to the bias line in the case of voltages in excess of some threshold. The current ATLAS-SCT sensors have punch-through protection (PTP) structures implemented. Nonetheless,

measurements with a large charge injected by a laser pulse showed that the strips can still be damaged [3].

In previous work, n-on-p strip sensors made by Hamamatsu with several different types of PTP structures implemented, were tested for ATLAS High Luminosity Upgrade studies [4]. The implant voltages of these sensors were measured with laser-based charge injection simulating the charge injection from 10^6 MIPs. The location of the charge injection was at the opposite ends of the strips, which have a PTP structure implemented only at one end (called “near”). It was found that for some of the PT structures the “near” implant potential was effectively limited irrespective of the location of the injected charge [5]. However, the voltages on the opposite end of the 1 cm long strip (called “far”) kept rising well above the 100 V objective. This difference is due to the fact that the large value of the implant resistance effectively isolates the “far” end of the strip from the PT structure leading to the large voltages.

We anticipate that this effect would be exacerbated for production sensors of the ATLAS High Luminosity Upgrade, since even the “short strip” concept of that design features 2.5 cm strips [6], which are longer than the 1 cm long test sensors we investigated.

To achieve a uniform surface protection for a sensor, a reduction of the implant resistance from the present 15 k Ω /cm down to at least 1.5 k Ω /cm would be necessary. As a first attempt, one

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would think that this could be done simply by a large increase in the implantation doses of the strips. Nevertheless, the difficulties with varying high doping concentrations are control of the electric field at the junction with the bulk silicon at the risk of very low sensor breakdown voltages; lattice damage in the implants; and the physical solid solubility limit of the dopants in silicon, which together with practical technological limits reach up to approximately $1 \times 10^{20} \text{ cm}^{-3}$, which is roughly the peak of the current doping profile.

As an alternative solution, the deposition of a conductive layer in contact with the strip implant was proposed. In this way, the PTP structures can be effective even when the large amount of charge is deposited far from the PTP side of the strip. An aluminum layer was deposited after the implant and before the coupling capacitor was formed. Contacts with the implant along the strip were formed. As the aluminum layer has a very low sheet resistance ($\sim 0.04 \Omega/\square$) a radical reduction of the strip resistance, down to $20 \Omega/\text{cm}$, was achieved.

2. Technology and fabrication

One batch of “low-resistance strip sensors” (LowR sensors) has been produced by the deposition of an aluminum layer in contact with the strip implants, reducing drastically the strip resistance. Later, the coupling capacitor was formed, using a specially deposited isolation layer, and a second metal layer. A cross-section of the critical part of the resulting strip can be seen in Fig. 1.

One of the technological challenges of this proposal is the creation of the coupling capacitor after the deposition of the first aluminum layer. These capacitors are called Metal–Insulator–Metal (MIM) capacitors. Thermal processes above about 400°C would destroy the aluminum. Therefore, the oxide deposition cannot be done at high temperatures. Obviously, the added metal layer also prevents the possibility of creating the oxide by the usual way of oxidizing the silicon underneath (thermal growth). The best technological option in this case is Plasma-Enhanced Chemical Vapor Deposition (PECVD). This technique allows the deposition of a layer of isolation material with sufficient quality at low temperature ($300\text{--}400^\circ\text{C}$). Nevertheless, there are concerns that this deposition method could result in an unacceptable pinhole density in the MIM capacitors.

In order to optimize the creation of the coupling capacitor, pretests with three types of MIM capacitors have been performed: (1) *Silane*: composed of 3000 \AA of SiH_4 -based silicon oxide (SiO_2) deposited in 2 steps; (2) *TEOS*: composed of 3000 \AA of TEOS-based (Tetraethyl Orthosilicate) oxide deposited in 2 steps; and (3) *Nitride*: composed of a tri-layer of $1200+1200+1200 \text{ \AA}$ of TEOS oxide + Si_3N_4 + SiH_4 oxide.

Tests have been performed on the different types of MIM capacitors fabricated in order to measure the CV characteristics, leakage current, breakdown voltage, and yield. Most of the parameters are very similar in all MIM capacitors fabricated, except for

the yield, which is considerably better for the “Nitride” case, as can be seen in Table 1. This result is expected, as the presence of 3 superimposed layers prevents intersecting pinhole production.

A first batch of LowR sensors has been produced at the Centro Nacional de Microelectrónica (IMB-CNM, CSIC), Barcelona, Spain, using the tri-layer deposited by PECVD for the MIM coupling capacitors. The PTP structures were defined between one strip edge and the bias rail, with a p-stop implant in between. In these sensors, the PTP structure was placed at the strip edge corresponding to the biasing resistor to make use of the “gate effect” provided by the polysilicon layer on top of the PTP area. A design of experiments (DOE) has been implemented in the design of the masks in order to optimize the PTP structure. Two parameters have been varied: the distance between N-implant and P-implant of the p-stop (s); and the p-stop implant width (p). These two parameters give the total PTP distance (d) as $d=2s+p$. The definition of these parameters and their values used in the DOE are shown in Fig. 2. An additional sensor with a very long PTP distance ($d=70 \mu\text{m}$; $p=8 \mu\text{m}$; $s=31 \mu\text{m}$) has been included as a reference for a sensor without a PTP structure implemented, so there is a total of 10 different sensors.

The sensors have 64 strips of about 2.3 cm length to be comparable with the proposed “short strip” sensors of the current ATLAS HL Upgrade prototypes. For each PTP geometry, there are two sensors on each wafer: one standard, with just 1 metal layer for the AC readout, and one of the LowR-type. Finally, some test structures and baby sensors have been added. A general view of the wafer layout can be seen in Fig. 3 together with a picture of one wafer.

Although the sensors were functional in the performance tests, the initial DC scans of PTP structures showed an unexpected behavior. It was not possible to measure the punch-through characteristic of the PTP as a breakdown of the oxide layer between the metallization and the poly-resistor appeared before a noticeable current flowed through the PT structure. This prevented us yet from making a full demonstration of the improvements in the beam-loss protection, as we cannot apply high voltages to the PTP structures. Nevertheless, dynamic tests have been done that indicate expected performance improvements of the new technology, as can be seen in the next section. Tests of other aspects of the sensor operation were done at normal operational implant voltage close to zero. They were not affected by this issue. This design deficit has been corrected in the next batch (results from it to be reported soon).

Table 1

Yield results for the C1 capacitor ($> 1 \text{ mm}^2$) in the 3 different types of MIM capacitors fabricated.

Yield [%]	Silane (%)	TEOS (%)	Nitride (%)
C1	81	86	94

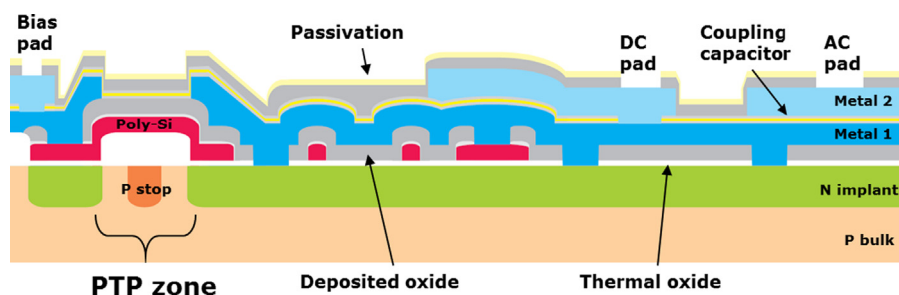


Fig. 1. Drawing of the cross-section of the LowR sensor strips.

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