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A simple digital delay for nuclear physics experiments

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ABSTRACT

A simple high precision digital delay for nuclear physics experiments was developed using fast ECL electronics. The circuit uses an oscillator synchronized with the signal to be delayed and a presettable counter. It is capable of delaying a negative NIM signal by 2 μs with a precision better than 50 ps. The circuit was developed for use in slow-fast coincidence units for Perturbed Angular Correlation spectrometers but it is not limited to this application.

1. Introduction

The use of high precision delays is common in nuclear physics apparatus, laser timing systems, and automated testing, amongst other applications. Perturbed Angular Correlation (PAC) of gamma radiation is a well-known nuclear physics technique for investigation in solid state physics through the measurement of hyperfine interactions [1]. PAC uses an unstable probe nucleus that decays through a γ–γ cascade, with an intermediate state with suitable spin, half-life, and nuclear moments. In a PAC spectrometer the time interval between the detection of the two γ transitions of the cascade is recorded; its histogram will show the half-life of the intermediate state of the cascade, perturbed by the interaction of the nuclear probe with the surrounding atoms in the material under study. The perturbation is extracted using standard procedures [2].

Although only two detectors are strictly necessary to detect the two radiations of the γ–γ cascade, virtually all PAC studies are currently performed using four- or six-detector spectrometers [2–11]. Digital signal processors started being used in the last decade [6–8,10,11] but the data rates are still challenging for this technical approach. Most conventional spectrometers use a “slow-fast” arrangement, schematically shown in Fig. 1 using only two detectors. Two signals are extracted from the photomultiplier associated with each detector: a fast signal from the anode, for timing, and a slow signal from one of the last dynodes, for energy discrimination. In the “slow-fast” arrangement the fast timing pulses after discrimination, typically using a constant fraction discriminator (CFD) [12], are gated by the corresponding slow energy channel. This arrangement has the advantage of reducing the number of events at the time-to-amplitude converter (TAC), but the delay introduced by the processing electronics in the slow channel must be compensated by a fixed delay inserted in the fast channel before the coincidence circuitry. An energy selection of the timing signals can also be achieved when detecting conversion electrons from one of the transitions of the γ–γ cascade of some PAC isotopes using a magnetic spectrometer or when using fast discriminators with energy selection [13–15] but these variants are less common.

A delay of about 1.5 μs is sufficient to ensure a good energy discrimination using a conventional amplifier with a short integration constant and a timing single channel analyzer (TSCA) for energy discrimination. This delay is usually done using 300 m of good quality coaxial cable which presents the following disadvantages:

- For a six-detector spectrometer this amounts to a total of 1800 m of cable occupying a larger volume than the rest of the electronics.
- To compensate for the degradation in amplitude and rise-time of the timing signal it is common to use an additional fast discriminator after the cable delay, thus increasing the number of electronic modules per detector channel; as an alternative the cable can be split in two sections, 200 m after the anode and 100 m after the CFD [4] which is not optimal for discrimination of the fast anode signals.

A simple delay circuit based on the well-known 74LS121 Transistor–Transistor Logic (TTL) monostable [16] with a selected

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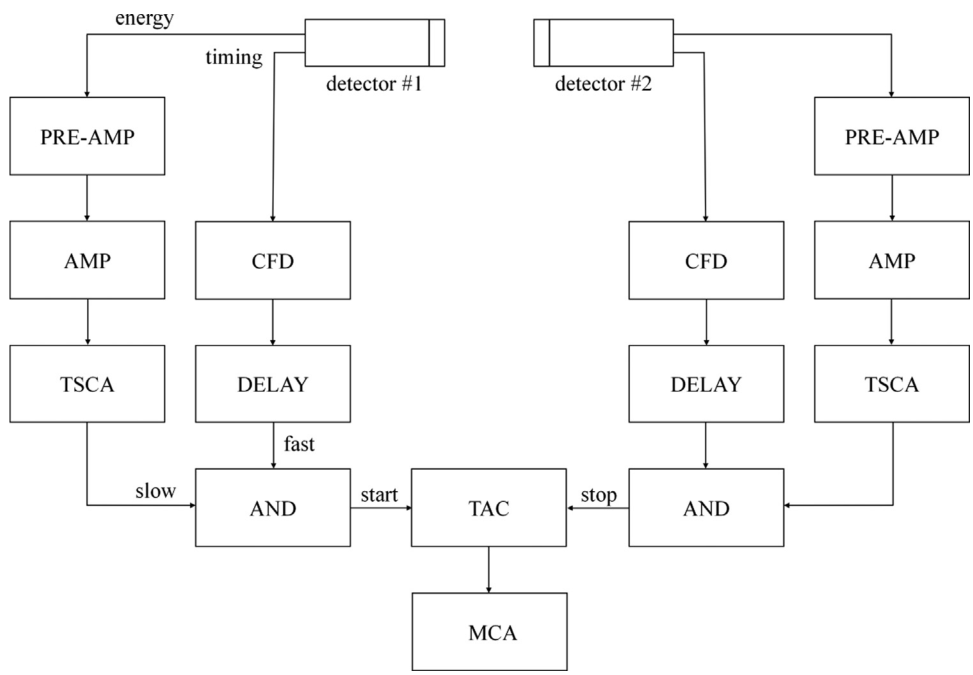

Fig. 1. Schematic representation of a "slow–fast" arrangement used in PAC spectrometers. Only two detectors are shown; when more detectors are used, the "start" input of the TAC is preceded by an OR logic function of all start signals from the detectors and the same is done for the "stop" signals; the memory of the multichannel analyzer (MCA) must then be subdivided in equal segments to include the necessary combinations of pairs of detectors.

capacitor has been used in a PAC spectrometer as an alternative to this procedure but the time resolution was limited to 1 ns for a delay of 1 μs [17], which was acceptable when measuring relatively slow hyperfine interaction frequencies using a spectrometer with NaI(Tl) scintillators. Since the typical time resolution using NaI(Tl) scintillators was of the order of a few ns, this active delay did not worsen the time resolution considerably. BaF_2 scintillators have been used in PAC spectrometers since the 1980s and allow time resolutions of the order of a few tenths of ns [18], also dependent on the energies of the γ–γ cascade [19]. Similar time resolutions can be achieved with the newer $LaBr_3$(Ce) scintillators [11] which have the added advantage of a better energy resolution than BaF_2. Thus fast, low jitter electronics are required and the number of units per detector channel should be reduced to the extent possible. The achievable precision for a state-of-the-art capacitor-based timing circuit can be inferred, e.g., from commercially available TAC, whose time resolution is specified at approximately 0.01% of the range [20,21], or 150 ps for a hypothetical 1.5 μs range.

The circuit discussed here is a simple alternative to the use of purely passive delay or to capacitor-based active delay. The delay introduced by a 300 m long cable is simulated using a significantly smaller cable and a control circuit which makes a signal go through the cable a certain number of times. This general approach has been implemented before using a 150 ns long cable and a programmable decade counter [22]. We have opted to insert the cable in an oscillator loop with simpler electronics and a significantly smaller cable. Surface mounted Emitter-Coupled Logic (ECL) circuits of the series 10H, 10E and 10EL (ON Semiconductor) [23,24] and an ultra-fast ECL comparator (Maxim) [25] were used in a multilayered board, achieving a 2 μs delay with a precision better than 50 ps.

2. Circuit description and implementation

The developed digital delay is based on an oscillator and a presettable counter. Since the signal to be delayed is random, if a free running oscillator was used it would be necessary to use a frequency of the order of a few GHz to obtain a precision of 100 ps, due to the inherent one-clock pulse error [26]. However, it is possible to use a frequency two to three orders of magnitude lower if a synchronous circuit is used, i.e., if the oscillator is started by the incoming signal. This approach has already been used with a crystal-controlled TTL oscillator [27], but its performance was still limited by the characteristics of TTL gates. Crystal-controlled oscillators using ECL gates are discussed in detail in Refs. [28,29]. These oscillators have very good stability to temperature and power supply variations which would make them the first choice for the application described here. However, we found it easier to make a reliable triggered oscillator using a simple cable delay in the feedback loop.

Fig. 2 shows a simplified diagram of the main part of the developed circuit, where filtering capacitors were left out. The incoming negative NIM [30] signal is first converted to ECL levels using an ultra-fast comparator (U1, MAX9691) and then triggers a D-type flip-flop (U2C, 1/4 of MC10E131). Any further incoming signals will be ignored until the delay period is over. Upon valid triggering, the Q* output of the flip-flop goes to the low state and enables a NOR gate (U3D, 1/4 of 10H102) to act as an inverter. With a 70 cm long (~3 ns) RG174 coaxial cable between the other input and the output, this gate will oscillate with a period of approximately 8 ns, i.e., twice the length of the cable plus the propagation delay of the gate. An oscillator synchronized with the incoming signal is thus obtained; its period can be adjusted using different lengths of cable. Practice has shown that a better performance of the oscillator is obtained using a gate with two independent outputs, so that one output is used only for the oscillator and the other only for the load; a second gate from the same chip is used as a buffer and the remaining gates are left unused, albeit properly terminated. The 50 Ω coaxial cable in the feedback loop is terminated using a standard 82.5–133 Ω resistor pair at the end of the cable to match its impedance [28].

An 8-bits presettable synchronous binary counter (U4, MC10E016) is used to count a prescribed number of times. In order to allow some flexibility, 4 bits can be programmed by the user via a dip switch and the remaining four are fixed. For the 3 ns long cable mentioned above the maximum delay is approximately 2 μs (256 times the oscillator period of 8 ns).