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Study of the directionality of cosmic muons using the INO-ICAL prototype detector

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ABSTRACT

The India-based Neutrino Observatory (INO) collaboration is planning to build a magnetised Iron-CALorimeter detector (ICAL) to study atmospheric neutrino oscillations with high precision. The ICAL adopts a 50 kton iron target and about 28 800 Resistive Plate Chambers (RPC) of 2×2 m^2 in area as active detector elements. As part of its R&D programme, a prototype detector stack composed of 12 layers of glass RPCs of 1×1 m^2 in area has been set up at the Tata Institute of Fundamental Research (TIFR) to study the detector parameters using cosmic muons. We present here a study of the capability of this prototype detector to distinguish between up-going and down-going muons.

1. Introduction

The INO-ICAL is a proposed neutrino physics experiment in India which aims to observe the neutrino oscillation pattern over at least one full period, to make a precise measurement of the neutrino oscillation parameters. This experiment will also focus on the determination of the neutrino mass pattern, the value of the leptonic CP phase and, last but not least, the search for any non-standard effect beyond neutrino oscillations. A detailed description of the INO project can be found in the project technical report [1]. RPCs will be used as active detectors in ICAL to detect charged particles produced by the interaction of neutrinos in the iron plates. During the R&D programme, three prototype detector stacks have been successfully built to study the performance and long-term stability of the RPCs using cosmic muons [2–4]. The work presented in this paper aims to characterise the capability of one of these stacks to distinguish between up-going and down-going muons, i.e., the directionality of the incident muons. For this purpose, it is important to understand the sources of time-offsets and their effects in defining the direction of the muons. The experimental data is also compared with a Monte Carlo (MC) simulation.

The paper is organised in the following manner: first the detector experimental set up (Section 2) is briefly discussed followed by the time delay measurement procedures (Section 3). Experimental results for muons directionality (Section 4) are then discussed. A MC study of muons timing (Section 5) is discussed afterwards and the results are compared with experimental data.

2. Experimental set up

The prototype stack (shown in Fig. 1) used in this study consists of 12 layers of glass RPCs of 1×1 m^2 in area. The layers are labelled serially from 0 (bottom) to 11 (top). Each RPC has two readout planes, labelled as X and Y, located on either side of it. Each plane has 32 strips with strips in the X plane orthogonal to strips in the Y plane. The width of the strips is 2.8 cm and the gap between adjacent strips is 0.2 cm. The layers are stacked on top of each other, separated by a distance of 16 cm, for a total stack height of 176 cm. Thanks to the good mechanical accuracy and by using alignment corrections derived by muon tracks, an overall position accuracy better than 1 mm is obtained [5]. The RPCs are operated in avalanche mode with tracking efficiencies in the central region of (95 ± 2)% at an applied voltage of 9.9 kV ($\pm$4.95 kV). The time resolution of these chambers is (1.2 ± 0.2) ns [6].

The flow of signals from the RPCs to the modules in the VME crate is shown in Fig. 2. Since the RPCs are operated in avalanche mode, the strip signals need to be amplified by a suitable factor using pre-amplifiers (here a gain of 80 was used). The length of cables going from the pre-amplifiers to the Analog Front End (AFE) boards is equal for all channels (1.7 m). The characteristic impedance of these cables is 50 Ω. Each RPC has a dedicated AFE and a Digital Front End (DFE) board (more detail in Refs. [7,8]). The AFE is equipped with adjustable threshold (up to 500 mV) discriminators and ECL output signals. The AFE also houses a trigger logic where the discriminator outputs of quadruplets of channels (0, 8,

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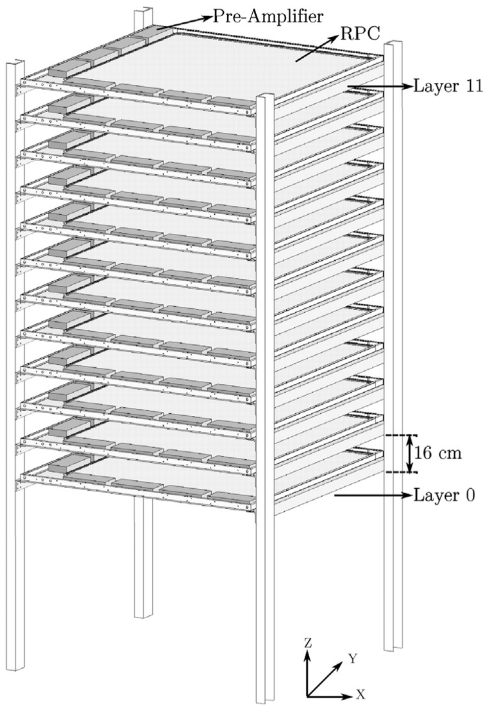

Fig. 1. Sketch of the prototype stack with 12 RPCs. Small rectangular shapes in each layer indicate the pre-amplifiers for the X- and Y-view.

16, 24; 1, 9, 17, 25; 2, 10, 18, 26; etc.) are shaped to 100 ns width and logically ORed to get eight level-0 trigger signals called T0 ($T0_0, T0_1, \ldots, T0_7$). The discriminated signals and the T0 signals then pass through the DFE, where the discriminated signals are first translated to TTL and stretched to a width of 700 ns.

The DFE board is composed of four sections:

- The Decoder unit which controls data acquisition and noise monitoring, uses the hand-shake signals from the Control and Data Router (CDR).
- The Event section which handles the latching of the strip-hit information. These latched data are flushed out serially to the CDR on receipt of an appropriate signal from the Decoder unit.
- The Pre-trigger section which generates level-1 trigger signals from different combinations of T0 signals (viz., 1-Fold, 2-Fold, 3-Fold, 4-Fold).[1] The timing measurement is made using the 1-Fold signals separately from the X and Y planes for each RPC.
- The Noise Rate Monitoring section which latches the noise rate of the active strip or calibration signal on receipt of a clock signal from the Decoder unit and switches over to the next strip. At the end of the cycle (32nd strip), the cycle is reset and the monitoring continues from the first strip. The clocking is handled by the data acquisition (DAQ) system.

The CDR routes the control signals and the data signals (Event Data/ Noise Rate Data) while the Trigger and Timing Router (TTR) routes timing signals to the back-end VME based DAQ system. A multi-hit TDC (V1190B-CAEN, 100 ps LSB) is used to record the timings. The strip hit information and the timing signal together constitute the event data. The event data is recorded by the DAQ system on receiving a trigger signal and the noise rate data is recorded on a periodic basis.

The trigger for the data collected for this study was generated by the coincidence of 1-Fold signals of four layers viz., the 2nd, 4th, 7th and 9th layer. In this study, we use approximately 2.1 million events acquired at an average trigger rate of about 22 Hz.

3. Measurement of the delay contributions of individual RPCs

Each stage of the electronic circuitry introduces its own delay which should be measured to get back the correct signal time. The first stage delay can be easily measured by knowing the muon hit position on the strip, whereas a particular effort is required to measure delays from stage 2 to stage 6.

3.1. Measurement with pulse generator

For preliminary studies, the calibrations were done using a pulse generator wherein a signal is simultaneously sent to two AFEs for two different layers among which one is the reference and the other is to be calibrated. With this method the time delay of stages 3–6 is measured while the delays of the readout strips and pre-amplifiers are not taken into account. The delays from RPC strips to the pre-amplifiers as well as from pre-amplifiers to the AFE inputs are equalised for all the channels using equal lengths of interconnecting cables. The 0th layer is chosen as the reference to calibrate other layers and the 1st layer is chosen as the reference to calibrate time delays for the 0th layer. A schematic of this calibration method is shown in Fig. 3. More details on the measurement procedure can be found in Ref. [6]. Using this method to calibrate the entire detector is cumbersome and time consuming. The results obtained using this method nonetheless give an idea of the order of magnitude of the delays. Fig. 4 shows the total time delay contribution from stage 3 to stage 6 of the individual strips (X-view) for two RPCs in the stack. A pattern is seen among strips i, $i+8$, $i+16$ and $i+24$ due to the fact that they are in wired-OR in the AFEs ('i' denotes here the strip number). The variation of time delay observed here between layer 0 and layer 8 is due to the particular choice of the reference layer.

3.2. Measurement with muons tracks

In view of the shortcomings seen in the method using the pulse generator, an alternative method is adopted using muon tracks as a source of timing calibration. The total time delay has been divided into two parts; the first comes from stage 1 (Fig. 2), which is due to the time delay in the RPC strips and the other part includes the time delays due to all electronics from stages 2 to 6. In order to measure the time delay in RPC strips, we consider events with single hit multiplicity and plot the time recorded in a particular RPC strip in the X-view against the Y coordinate of the firing strip in the Y-view. A linear fitting of time vs. hit here provides the time delay in the RPC strips which is found to be (4.8 ± 0.2) ns/m. An approximate value of 5 ns/m is considered in the following for the analysis. The raw TDC timing is first corrected by the time delay due to RPC strips and then used to determine the time delays from the stages 2 to 6 using this formula:

$$t_i = \delta + \frac{1}{c} l_i \tag{3.1}$$

where, t_i is the relative time of ith layer with respect to the lowest layer with a valid hit and l_i is the corresponding cosmic muon track length. The only free parameter in this fitting, the intercept (δ) has to be estimated using the track length, timing information from other layers as shown in Eq. (3.1).

Signals from all 32 strips for one side of a RPC are ORed in the AFE and DFE board which generate the final 1-Fold trigger signal

[1] 1-Fold=$T0_0 + T0_1 + T0_2 + T0_3 + T0_4 + T0_5 + T0_6 + T0_7$, 2-Fold=$T0_0 \cdot T0_1 + T0_1 \cdot T0_2 + T0_2 \cdot T0_3 + T0_3 \cdot T0_4 + T0_4 \cdot T0_5 + T0_5 \cdot T0_6 + T0_6 \cdot T0_7$ and so on. Here, '+' means OR and '·' means AND. This 1-Fold signal is the timing data for a layer.