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Beam test results of pixel triggerless prototypes for the $\overline{\text{P}}$ANDA MVD

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ABSTRACT

Hybrid pixel and double sided silicon microstrip devices will equip the Micro Vertex Detector of the $\overline{\text{P}}$ANDA experiment. The most challenging request of the experiment is the continuous readout at the rate of 2×10^7 interactions/s. The detector is in an advanced R&D phase and pixel assemblies, composed of thinned epitaxial sensor read out by the custom chip prototype ToPix, developed in the 130 nm CMOS technology, were produced. The triggerless ASIC implements readout channels that are able to detect signals and transmit the information with a precise timestamp. It performs the energy loss measurement using the Time over Threshold technique, in the input range to about 50 fC. A dedicated testing bench allows the control and the readout of each single chip assembly. Two experimental setups were assembled for testing these first single chip prototypes with pions at CERN, T9, in August 2012. The first one is based on a pixel assembly positioned in the middle of a telescope composed of double sided silicon strips sensors. A 50 MHz clock signal synchronizes these two systems, the triggerless pixels and the strip detectors triggered by scintillation detectors. The second experimental setup is a tracking station housing four pixel assemblies. First results will be reported.

1. Introduction

At the Facility for Antiproton and Ion Research (FAIR) in Darmstadt, the High Energy Storage Ring (HESR) [1] will make available antiproton beams of unprecedented quality in the 1.5−15 GeV/c momentum range. The fixed target experiment $\overline{\text{P}}$ANDA [2] will occupy one of the two straight sectors and it will make use of these cooled antiproton beams colliding on hydrogen or heavier nuclei. The spectroscopy of charmonium, the search of exotic states and the study of strange physics will be the main physics topics [3]. Primary and secondary vertexes reconstruction of short lived particles is crucial for precise measurement in the charm quark energy region. The Micro Vertex Detector (MVD) of the experiment has to cope with this challenging task and has to achieve a spatial resolution better than 100 μm. In addition to the good spatial resolution, limited material budget, radiation hardness, contribution to the global particle identification by energy loss measurement and support to particle momentum evaluation are common requirements to vertex detectors. Because of the absence of the hardware trigger and of the high rate of about 2×10^7 interactions/s, the request of a continuous data transmission is a challenge. In proton–antiproton collisions, a high track density in the forward direction is obtained because of the Lorentz boost; therefore 6 disks composed of hybrid pixel detectors will equip this region. In addition, two double sided silicon microstrips rings will be arranged at the outer radius of the two last disks. In case of antiproton–nucleus interactions, the emitted particles are distributed over higher polar angles; four barrels arranged around the interaction point will cover this region of the MVD. The inner layers are composed of hybrid pixels and the outer ones are based on double sided microstrips. The detection polar angle ranges from 3° to 150°; the interface between disks and barrels is located at 40°. Pixel detectors were chosen to equip the innermost layers of the MVD because of their unambiguous 2D readout, the capability of double hit resolution and an excellent signal to noise ratio at high speed. The pixel detectors are based on the standard hybrid technology, which has been reliably used at LHC experiments; in this technology, both electrical and mechanical connections between the sensor and the readout chip are achieved by means of solder balls in a flip-chip solder-bonding process. The size of the pixels is a trade-off between the physics requirements and the space constraints in order to include all the electrical features; a cell

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size of 100 μm × 100 μm was therefore chosen. A readout ASIC in 130 nm CMOS technology is being developed for this purpose. Furthermore, to cope with the limited material budget an R&D effort to investigate a lower sensor thickness has been pursued. References [4,5] indicated that silicon epitaxial material could be suitable to be applied in the PANDA MVD. Its radiation tolerance and the capability to operate at room temperature will allow for the use of a simple cooling system.

2. Single chip pixel assembly

The design of the MVD is ongoing and the R&D is in a very advanced phase with the production of the first single chip pixel assemblies. They are composed of thinned epitaxial silicon sensors (down to 100 μm of thickness) read out by the ASIC prototypes named ToPix_3. The first characterization of these thinned assemblies featuring triggerless readout was performed with the beam test at T9 of CERN, in August 2012.

2.1. ToPix_3 prototype

ToPix_3 is a reduced scale prototype [6] providing spatial, time and energy information of the incoming particle. The energy loss measurement is obtained using the Time over Threshold (ToT) technique which keeps a good linearity for charges up to 50 fC. It includes two 256-cells double columns and two 64-cells double columns. The longer columns are folded to four 32-cells sub-columns in order to have an almost square form factor, obtaining a $4.5 \times 4\ mm^2$ chip size. The complete pixel cells, the end of column control logic and buffer circuits were implemented, while the output multiplexer and serializer are still in a simplified revision. Bump bonding pads have been used in the pixel cells for direct connections to the sensor. Digital input and output e-links use differential SLVS [7] standard in order to reduce the digital noise contribution and to be compatible with the 1.2 V power supply. A constant current discharges the feedback capacitance of an integrator. The start and stop times of the discharge, as intercepted by a comparator threshold, are measured by latching into local registers Gray-encoded words provided by a counter which is common to all channels. The start time corresponds to the leading edge information, and the relative stored word is the timestamp of the detected hit, while the stop time corresponds to the trailing edge information. The time difference between them, measured in clock cycles, is the Time over Threshold information; the response is linear even when the preamplifier is saturated. The characterization of this chip showed a final baseline dispersion of about 65 electrons after the correction using the on-pixel 5 bit DACs. A noise of about 100 electrons was measured without the detector. Additional results concerning ToPix_3 are reported in the MVD's TDR [8].

2.2. Epitaxial silicon sensor

A dedicated sensor was designed to match exactly the 640 readout cell matrix of ToPix_3, with a final layout of 32 rows times 20 columns. On the sensor perimeter, the guard ring sequence foresees the first one connected to ground and the outer ones floating. The active part of the sensor is an epitaxial silicon layer; this material was selected for its good radiation tolerance, as reported in Ref. [9]. Blank epitaxial silicon wafers were delivered by ITME (Warsaw) and p-in-n pixels were manufactured by FBK (Trento). The thinning of the Czochralski (Cz) substrate down to 20 μm and bump bonding processes were performed at IZM company (Berlin). Each pixel features a 100 μm × 100 μm size matching the readout cell of ToPix_3. The Sn–Pb bump pads are arranged in a mirror configuration with respect to a bus serving two adjacent pixel columns. The thin Cz layer is the ohmic contact for the sensor biasing on the sensor backside, without additional aluminum deposition process. The bump bonding yield of seven tested assemblies is not lower than 99.5%.

2.3. Test bench of the assembly

Each assembly is wire bonded to its testing board (Fig. 1) which is connected to a Xilinx evaluation board housing a Virtex 6 FPGA. The control and acquisition programs are developed in a LABView framework.

3. Experimental setups

One pixel assembly was installed in the middle of a telescope (Fig. 2) composed of 4 planes, each equipped with a double-sided micro strip sensor featuring 1.92 cm × 1.92 cm active area, 50 μm pitch and 285 μm thickness [10,11]. Each sensor is readout with six APV25 chips, each of them bonded to 128 strips.

The telescope planes can be translated along the particle beam direction, while the pixel assembly can rotate around the pixel matrix axis. The strip acquisition is triggered by a coincidence of two scintillator stations arranged in front and behind the telescope. The triggerless pixel detectors and the strip data acquisition system are synchronized by a 50 MHz clock signal. This guarantees the timestamp

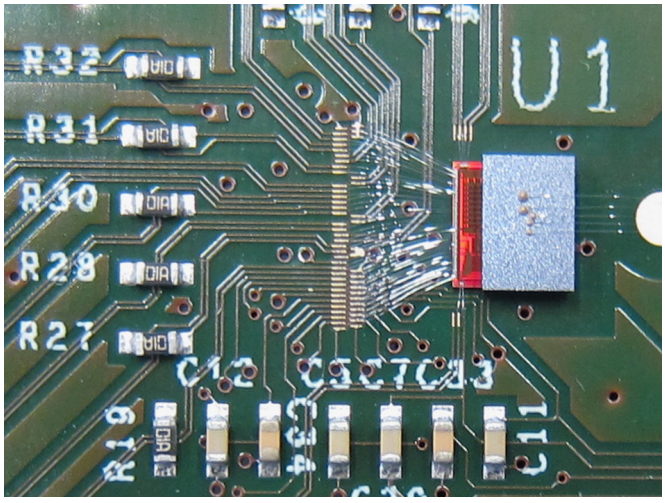

Fig. 1. Single chip assembly. On the left side of the assembly (right part of the picture) the chip is visible with its wire connections to the testing board pads. The sensor covers the most of the prototype and its biasing is obtained using wires directly bonded to the Cz backside.

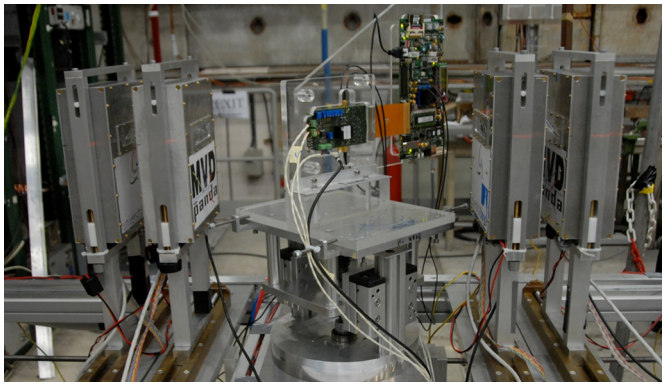

Fig. 2. Pixel test bench positioned on a rotation support in the middle of a silicon strip telescope.