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Development of CdTe pixel detector for synchrotron radiation experiments

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ABSTRACT

This study describes the development of a CdTe pixel detector for high-energy X-ray diffraction experiments at synchrotron radiation facilities. We have developed three prototypes. The third prototype detector (SP8-02B) was designed with a pixel size of 200 μm × 200 μm and a matrix of 20 × 50 pixels. The sensor was bonded to an application-specific integrated circuit with a preamplifier, shaper, window-type discriminator, and a 20-bit counter for each pixel. The SP8-02B detector improved the uniformity between pixels in one chip in comparison with the previous prototypes. The long-term stability was measured at various temperatures. A moderate cooling achieved good stability that was not affected by the polarization effect.

1. Introduction

Super Photon ring-8 GeV (SPring-8) [1] provides high-brilliance synchrotron radiation (SR) beams over 100 keV, which provides a powerful probe for analyzing the deep inner structures in a heavy material. In particular, high-energy X-ray diffraction (XRD) experiments are the most important experiments in SPring-8. The typical energy range of XRD is from 10 keV to 30 keV, whereas transmission geometry XRD [2] employs much higher energies.

Single-photon-counting pixel detectors with silicon sensors are widely applied in SR experiments. The PILATUS detector provides a large dynamic range, fast data readout, and a low-noise performance compared with a conventional CCD detector or imaging plate [3,4]. However, since PILATUS employs silicon sensors of 320 μm thickness, its detection efficiency for X-rays is only 10% at 30 keV and 1.4% at 100 keV. Therefore, we have developed a new single-photon-counting pixel detector with a cadmium telluride (CdTe) sensor. CdTe has a high atomic number as well as a high density, which results in a much higher detection efficiency. For example, a CdTe sensor of 500 μm thickness could achieve a detection efficiency of 100% at 30 keV and 45% at 100 keV.

The first prototype detector (SP8-01) was designed with a pixel size of 200 μm × 200 μm and a matrix of 16 × 16 pixels [5,6]. The application-specific integrated circuit (ASIC) of SP8-01 had a preamplifier, shaper, window-type discriminator with offset trims, and a 20-bit counter for each pixel. SP8-01 was successfully operated as an X-ray detector in photon-counting mode in the energy region of 15–100 keV, where the dependence of the photon energy with respect to the threshold voltage was found to be linear [6]. The low threshold and high threshold of the window comparator are used to remove electronic noise and fluorescent X-ray background, and higher-harmonic beam contamination respectively. In the second prototype SP8-02 was 3-side buttable with 20 × 50 pixels and an excellent bonding yield was achieved with no dead pixels [7]. Using these prototype detectors the basic properties of a CdTe detector for a fast counting device were obtained.

However, the threshold energies of the discriminator differed greatly from one pixel to another in SP8-02 because of the baseline irregularity of the shaper output. The baseline dispersion was as high as 325 mV, which corresponds to 78 keV in a typical setting. In addition, the offset trim in one pixel affected the threshold in other pixels. This meant that the offset trim was almost impossible to adjust.

SP8-02B was developed as the third prototype detector. The main objective of SP8-02B was to suppress the dispersion of threshold energies of the discriminator. In this paper we present the specification of SP8-02B in Section 2, the performance of the prototype in SR experiments in Section 3 and concluding remarks as well as future plans in Section 4.

2. Specification of SP8-02B

Table 1 shows the main specifications of the sensor for SP8-02B. In the previous study a Pt/CdTe/Al-pixel sensor was operated

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as a Schottky diode detector in electron-readout mode [7]. We fabricated a CdTe sensor for SP8-02B with Al Schottky contacts on the pixellated side. The pixel size and the positions of the bumping pads were kept the same as SP8-02. In this way, it was not necessary to modify the existing CdTe sensor. This shortened the development period of the SP8-02B prototype detector. Au/In stud bonding technology [8] was employed to bond the CdTe sensor to the readout board.

A full-custom ASIC was designed for SP8-02B readout and fabricated with the TSMC 0.25 μm CMOS process [9]. Fig. 1 shows the block diagram of the readout circuit in one pixel. It has a preamplifier, pole-zero circuit, shaper, offset trim, window-type discriminator, and a 20-bit pseudo-random counter. The specification for SP8-02B is shown in Table 2 together with the specification for SP8-02.

The equivalent noise charge (ENC) was lowered by optimizing the preamplifier and shaper. To suppress the dispersion of the baseline levels, the design of the pole-zero circuit was improved, and an auto-offset-canceller was added to the shaper.

Table 1
Specifications of the CdTe sensor for SP8-02B.

Material	CdTe
Thickness	0.5 mm
Pixel size	200 μm × 200 μm
Matrix of chip	20 pixel × 50 pixel
Bump-bonding	In/Au stud bonding
Contact of sensor	Pt on bulk side
	Al Schottky on pixellated side

The digital-to-analog converter (DAC) in the offset trim is the differential design in SP8-02B. This prevents to affect the threshold levels of the discriminator of other pixels. The offset trim in SP8-02B has one 6-bit DAC, whereas SP8-02 had two DACs per pixel. In SP8-02, there were 6- and 7-bit DACs for higher and lower-energy thresholds, respectively. Instead of adjusting each of the threshold voltages, as it was done in SP8-02, an offset trim circuit was added at the shaper output. In this way, it is possible to set nearly the same energy range for all the window-type comparators. The advanced pole zero circuit and the auto-offset canceller require more space than the designs used in the previous ASIC. The required additional space was freed by removing one of the trim DACs.

The dispersion of the baseline levels is difficult to estimate using a simulation program. For this reason the step of the DAC was designed to be variable and allows the dispersion of the baseline levels to be suppressed by as much as 1/63.

The previous ASICs were able to collect both positive and negative charge signals. The readout for SP8-02B is required to operate in a negative charge collection mode only. Therefore, SP8-02B is optimized only for a negative charge collection mode, and the higher-energy threshold of the window-type comparator is valid only for signals from negative charges. This also helped to keep the circuit size down to 200 μm × 200 μm.

3. Performance of SP8-02B

3.1. Setup for the performance test

A test board was developed for SP8-02B. Fig. 2 shows SP8-02B in a testing setup. The SP8-02B was wire bonded to a ceramic

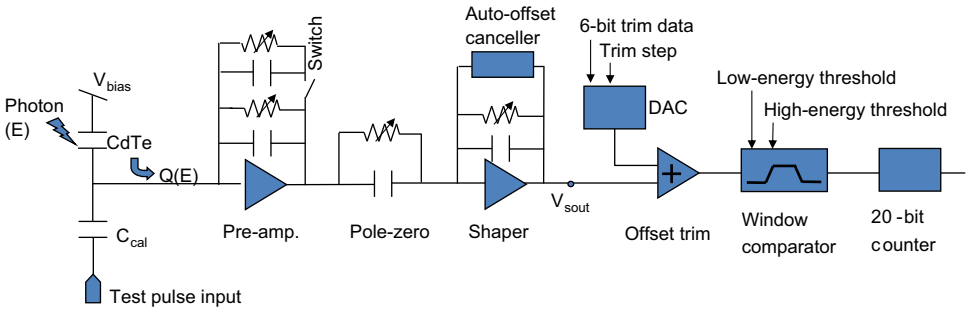

Fig. 1. Schematic diagram of readout circuit in one pixel.

Table 2
Comparison of designed specifications of SP8-02B and SP8-02 ASICSs.

	SP8-02B	SP8-02
Pixel size	200 μm × 200 μm	200 μm × 200 μm
Matrix of chip	20 pixel × 50 pixel	20 pixel × 50 pixel
Readout charge	Negative charge	Positive or negative charge
Preamplifier	Charge sensitive amplifier with a gain switch low-noise design	Charge sensitive amplifier with a gain switch
Energy range	15–40 keV (high gain)	15–40 keV (high gain)
	30–100 keV (low gain)	30–100 keV (low gain)
Pole-zero circuit	Advanced	Simple
Shaper	With auto-offset-canceller	Without auto-offset-canceller
Peaking time	100 ns	100 ns
Offset trim	6-bit to adjust offset of signal line	7-bit for lower-energy threshold
		6-bit for higher-energy threshold
	Differential output	Single-end output
	Step variable	Fixed step (5 mV/bit)
Comparator	Window-type comparator	Window-type comparator
	Valid for negative charge	Valid for positive or negative
	Signals	Charge signals
Counter	20-bit pseudo-random counter	20-bit pseudo-random counter
ASIC process	TMSC 0.25 μm CMOS	TMSC 0.25 μm CMOS