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Frontend electronics development for the CMS pixel detector upgrade

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ABSTRACT

The performance of the LHC accelerator at CERN has been outstanding since its startup in 2010. It seems likely that the delivered instantaneous luminosity exceeds its design value of 10^{34} cm^{-2} s^{-1} soon after the recommissioning in 2015. Tracking in such a dense environment is challenging. In order to compensate for the expected decrease in performance due to the high number of simultaneous interactions, an upgrade of the pixel detector has been proposed. Limitations of the frontend electronics of the present system are discussed and it is shown how they will be overcome.

1. Introduction

The LHC accelerator is expected to reach about twice its design luminosity before the 2nd long shutdown in 2018. The CMS collaboration will replace the entire pixel detector around 2016 with an upgraded device [1–3]. The barrel part of the detector will be supplemented by a fourth layer at a mean radius of 160 mm. The innermost layer is moved closer to the interaction region by 10 mm resulting in a mean radius of 30 mm. A third endcap disk on each side will be added. In order to cope with the substantial increase in data rates, an improved version of the frontend electronics is needed.

Fig. 1 shows a drawing of a sensor module of the outer barrel layers. Modules of the other parts of the detector differ mostly by the way they are mounted and by the cables used. From top to bottom one can see the cables with a connector print, the High Density Interconnect with a module controller ASIC called Token Bit Manager (TBM) mounted in the center, the silicon pixel sensor, 2×8 readout chips (ROC) and base strips for mounting. While most components are modified, this paper focuses on the changes to the main electronics components, the ROCs and the TBM.

2. Readout chip

The ROC (psi46dig) for the upgraded detector is not a completely new development but rather an evolution of the well-proven ROC (psi46v2) operating in CMS since its commissioning [4]. It is designed in the same 250 nm CMOS technology and the well understood core of its architecture is mostly unaltered.

In order to adapt the ROC to the new requirements the limitations of the psi46v2 have to be understood. Several areas which need modifications have been identified:

(i) *Digital readout:* To cope with the higher data bandwidth the readout protocol has been changed from a 40 MHz analog to a 160 MBit/s digital readout [5]. An ADC digitizes the analog pulse height information in the ROC periphery (see Fig. 2). The key elements are an 8-bit successive approximation current ADC running at 80 MHz with a programmable range and a PLL which generates the 160 and 80 MHz for the serial readout links and the ADC respectively, from the 40 MHz LHC master clock. Both circuit blocks have been prototyped and tested in a previous multi project submission. The ADC shows a non-linearity within the last bit in the full range. The PLL has an extremely wide locking range between 10 and 75 MHz. Its voltage controlled oscillator ranges up to 530 MHz and showed a decrease of 10% after a γ-irradiation of 50 Mrad. This ensures a frequency range wide enough for operation after the radiation induced damage expected over the full detector lifetime.

(ii) *Reduction of data loss:* The pixel hit data has to be stored inside the ROC during the level 1 trigger decision time (≈4 μs). The size of the buffers has been optimized for the barrel layer at 4 cm and the LHC design luminosity. They need to be increased substantially. The psi46dig ROC has 26×80 data buffers (compared to 26×32 in psi46v2) and 26×24 time stamp buffers (26×12). To limit the increase of the area used by the buffers the layout has been redone completely.
To further reduce data losses an extra readout buffer stage has been introduced in the ROC periphery of psi46dig as shown in Fig. 3. To understand the need for this, one has to look at the readout architecture of psi46v2. The ROC is organized in 26

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double columns with 160 pixels each. Once a double column has trigger validated data in its buffers it stops data acquisition until it has been read out. The readout uses a serial protocol, where all double columns and all (or half of the) ROCs in a module are daisy chained. It is controlled by a readout token bit generated in the TBM (hence the name). The higher the link occupancy the longer is the readout time and hence the dead time in the columns. To reduce the waiting time for the readout token, in psi46dig the data is transferred (after being digitized) into the new readout buffer immediately after the trigger arrives and the double columns go live again. This is done in parallel in all ROCs of the module by virtue of a token bit generated in the ROC itself. A second external readout token bit from the TBM then controls the module readout. This does not introduce an additional dead time, as long as the readout buffer is not filled up. Depending on position and instantaneous luminosity the related dead-time can be reduced from 3 to 4% to below 1%.

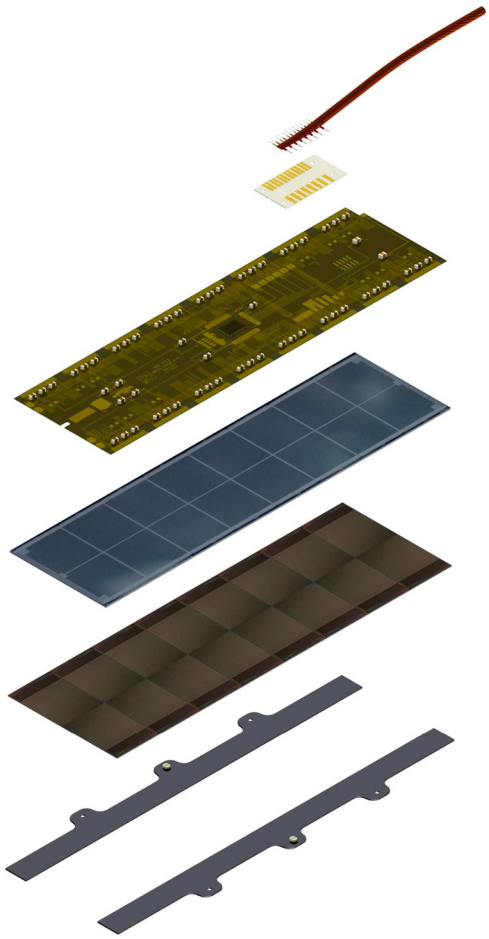

Fig. 1. Drawing of digital sensor modules for the outer barrel layers.

(iii) *Analog performance:* A key parameter of the ROC is its lowest achievable charge threshold in the pixel. The lower it is the longer is the lifetime of the detector. This is because after high irradiation doses the sensor will eventually be operated in a non-fully depleted mode and the charge collection efficiency decreases. Therefore a lot of effort went into an improved performance of the analog amplifier and the discriminator in the pixel unit cell. A very detailed simulation of the passive power distribution including important parasitic elements indicated where possible signal crosstalk could occur. Consequently, the power distribution in the ROC has been optimized. The power rails feeding the very noise-sensitive circuit parts have been more effectively decoupled from the noisy digital power rails. Rerouting of some critical wires was needed and an additional and thicker metal layer has been used.

But even a low absolute charge threshold does not guarantee a low practical (or in-time) threshold, because of timewalk of the discriminator. In the present ROC there is a difference between absolute and in-time threshold of 700 e^-. The charge discriminator has been redesigned to improve the timewalk behavior. Fig. 4 shows the lab measurements. Absolute thresholds below 1.8 ke^- are possible (2.5 ke^- for the present ROC) and there is no measurable increase of practical threshold due to timewalk. The most probable charge deposition for a minimum ionizing particle is about 21 ke^-.

(iv) *Operational issues:* Several minor changes have been implemented, which will facilitate the operation of the detector. For instance a power-up reset circuit is introduced to ensure a low power state of the ROC after powering on. Programmable parameters on the ROC have been made independent of each other as far as possible to simplify procedures of finding ideal settings after radiation damage. Other programmable features have been removed since it turned out that they are not needed.

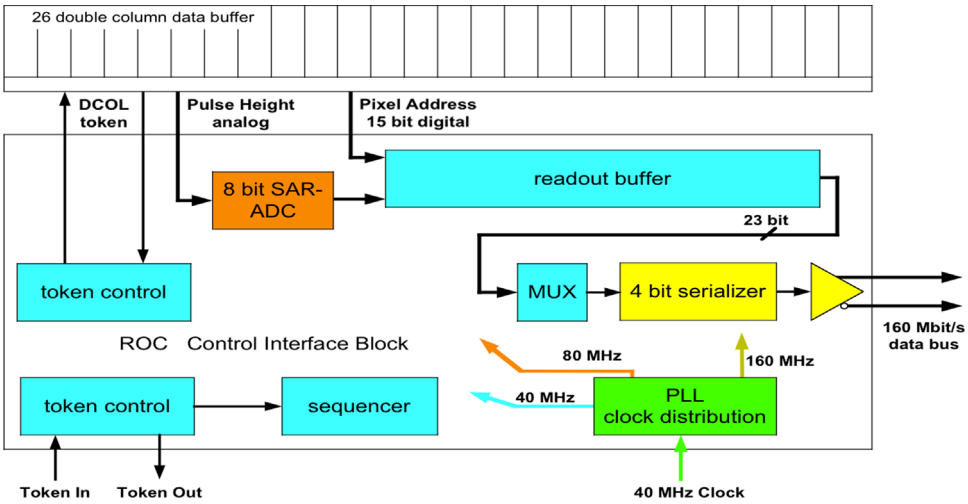

Fig. 2. Schematic view of the ROC periphery. These circuit blocks were different or not present in the psi46v2 ROC.