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3D integration of Geiger-mode avalanche photodiodes aimed to very high fill-factor pixels for future linear colliders

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ABSTRACT

This paper presents an analysis of the maximum achievable fill-factor by a pixel detector of Geiger-mode avalanche photodiodes with the Chartered 130 nm/Tezzaron 3D process. The analysis shows that fill-factors between 66% and 96% can be obtained with different array architectures and a time-gated readout circuit of minimum area. The maximum fill-factor is achieved when the two-layer vertical stack is used to overlap the non-sensitive areas of one layer with the sensitive areas of the other one. Moreover, different sensor areas are used to further increase the fill-factor. A chip containing a pixel detector of the Geiger-mode avalanche photodiodes and aimed to future linear colliders has been designed with the Chartered 130 nm/Tezzaron 3D process to increase the fill-factor.

1. Introduction

Vertically integrated circuits (3D-ICs) are a very promising alternative for silicon pixel detectors aimed to High Energy Physics (HEP) experiments at future particle colliders. The potential of 3D technologies lies in the fact that they allow to achieve higher densities of integration without using nanometer technologies, which complicate the design of analog circuits and suffer from high technologic dispersions. Another advantage of 3D-ICs is that they also allow the separation of functional blocks (sensor, analog and digital) into different layers [1]. Moreover, there exist groups working with the traditional HEP hybrid pixel approach in 3D (ATLAS effort for 3D integration) with the goal of reducing the pixel size while keeping the 130 nm feature size. 3D technologies can also be used to increase the fill-factor of GAPD (Geiger-mode Avalanche PhotoDiodes) detectors, which rarely exceeds 10% when fabricated in conventional 2D technologies. Amongst other challenging requirements, a 100% fill-factor is demanded by future linear colliders on detector systems [2].

In this paper, a GAPD pixel array aimed to particle tracking/vertexing in future linear colliders and fabricated in a 3D process to maximize the fill-factor is presented. The paper is organized as follows. Section 2 describes the principle of operation of GAPDs, their main problems and known solutions. Section 3 introduces the Chartered 130 nm/Tezzaron 3D process. Section 4 presents the detector architecture as well as an analysis of the achievable fill-factor with the Chartered 130 nm/Tezzaron 3D process. Section 5 summarizes the conclusions.

2. Geiger-mode avalanche photodiodes

In conventional CMOS technologies, GAPDs are generally implemented by means of a simple p^+/n-well junction and biased above the breakdown voltage (V_{BD}) to operate in the Geiger-mode [3,4]. At this polarization, an electric field of the order of 10^6 V/cm is created in the depletion region. Upon absorption of impinging radiation within the depletion region, e^-–h^+ pairs are generated. These e^-–h^+ pairs can be accelerated by the high electric field up to the point at which they can in turn generate other e^-–h^+ pairs by impact ionization. The new pairs can be accelerated as well and generate more pairs also by impact ionization, thus starting an avalanche multiplication process that gives rise to a macroscopic current pulse in picoseconds. This current pulse can be detected and digitized by the readout electronics. However, since the avalanche is self-sustaining, the current continues to flow and it needs to be stopped in order to avoid self-heating or even burning the sensor. This operation is performed by the quenching electronics by lowering the reverse bias voltage down to or below V_{BD}. Once the avalanche has been quenched, the GAPD returns to its original state (i.e. it is polarized again) so that the sensor is made sensitive again for upcoming particles.

In contrast with other sensor technologies that are also being developed for future linear colliders, GAPDs enable single hit detection at each BX (Bunch Crossing) thanks to their extraordinary sensitivity and picosecond rise times. In spite of these advantages, GAPDs suffer from two main problems. First, there

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exist noise pulses, which cannot be distinguished from radiation triggered events and thus worsen the detector occupancy and SNR (Signal-to-Noise Ratio). These fake pulses, expressed in counts per second (Hz), are generated by dark counts, after-pulses and cross-talks. Dark counts are spurious pulses due to thermal and band-to-band tunneling carriers within the junction. After-pulses and cross-talks are correlated noise pulses. After-pulses are generated when carriers captured by trapping centers during an avalanche flow are released after the sensor has recovered its polarization condition. Cross-talks are fake pulses which appear when an avalanche in one pixel triggers a secondary avalanche in a neighboring pixel. Usual noise frequencies range from a few kHz to tens of kHz. Second, the fill-factor of GAPDs is too low. It rarely exceeds the 10%, which results in a low detection efficiency. Such a reduced fill-factor is due to two aspects of the design of the pixel, which are the non-sensitive areas of the sensor and the readout electronics. The non-sensitive areas of the sensor include the guard ring surrounding the p^+/n-well junction. Additionally, in deep-submicrometer technologies, the masks that the designers introduce in the layout to block the Shallow Trench Isolation (STI) also create non-sensitive areas. In a conventional CMOS process, the diode geometry creates a higher electric field at the edges, which leads to premature edge breakdown. To avoid this unwanted effect, the junction of the diode is surrounded by a guard ring with a lower doping profile. However, the guard ring usually is non-sensitive. In addition, for those technologies below the 0.25 μm node, a SiO_2 STI is compulsorily constructed in the fabrication process to prevent punch-through and latch-up. Punch-through is the existence of a parasitic current path located below the gate which shorts the drain and source terminals of CMOS transistors. Latch-up is the inadvertent creation of a low-impedance path between the high and the low power supply terminals of CMOS circuits. Both phenomena increase the power consumption and therefore they must be avoided. Nevertheless, the presence of the STI near the GAPD depletion region may induce extremely high levels of noise at frequencies above several MHz [5]. Fortunately, there exist several design techniques at the layout level to force the physical separation of the STI interface from the GAPD depletion region and obtain a beneficial impact on the noise, but at the expense of reducing the fill-factor [6–8]. The readout electronics is also monolithically integrated with the sensor on the same die to improve the dynamic response. Even though readout circuits based on a simple voltage comparator and a memory element are typically used, and thus with a small number of transistors, the area occupied by the transistors is still too large when compared to the sensor area. As a result, the non-sensitive area of the pixel chip is quite large compared with the sensitive area.

The noise issue can be handled with using advanced techniques, such as the time-gated operation or particle sampling at various layers. The GAPD detector presented in this work is operated in time-gated mode [9]. In this regime of operation, the sensor is periodically activated and deactivated under the command of a trigger signal to reduce the probability of detecting noise pulses that interfere with the radiation triggered pulses. Moreover, thanks to the trigger command, the active periods of the sensor can be synchronized with the BXs of the accelerator in order to avoid missing any real hits. As a result, the SNR and Dynamic Range (DR) of the sensor can be increased by several orders of magnitude [10]. Nevertheless, it is difficult to increase the fill-factor with standard CMOS technologies. In this work, the 3D vertical integration of a two-layer chip is proposed as a solution to overcome the fill-factor limitation of GAPD devices.

3. 3D vertical integration with the Chartered 130 nm/Tezzaron process

The 3D GAPD detector described in this work is in a 130 nm CMOS process fabricated by Chartered Semiconductor and vertically integrated by Tezzaron, available in MPW (Multi-Project Wafer) runs. 3D-ICs manufactured in the Chartered 130 nm/Tezzaron 3D process, typically consist of two layers of logic dies fabricated by Chartered Semiconductor and two or (if possible) three layers of memories supplied by Tezzaron. However, it is also possible to build a two-layer stack with no memories attached (no-DRAM option), which is the case with this work.

In this option, the 3D-ICs are manufactured by independently fabricating the 2D logic dies corresponding to the two different layers (called tiers) on separate wafers. Then, the two wafers are stacked face-to-face, bonded together, thinned, and finally diced [11]. During the bonding process, the top of the WTOP wafer is flipped onto the top of the WBOTTOM wafer in a right-to-left orientation. Hence, the two logic dies are connected face-to-face (wafer-to-wafer). The connection between tiers for relaying signals is made through Metal 6, which is the highest metal of the technology process. This 3D process also uses via-first Through Silicon Vias (TSVs) for connection between the logic circuitry and the I/O bond pads, which are placed on the back of the WTOP tier. TSVs are also used to control thinning. As a consequence, it is necessary to maintain a minimum TSV density throughout both tiers, which forces the utilization of dummy TSVs. The recommended TSV pitch is 100 μm. TSVs are arranged in an hexagonal shape and covered with Metal 1. After bonding, the WTOP wafer is thinned down to about 12 μm until the bottom ends of the TSVs are exposed. The WBOTTOM wafer can also be thinned, however this incurs additional costs. Back metal for bonding pads is applied to the thinned WTOP wafer. When all this processing is done, the wafer stack is diced.

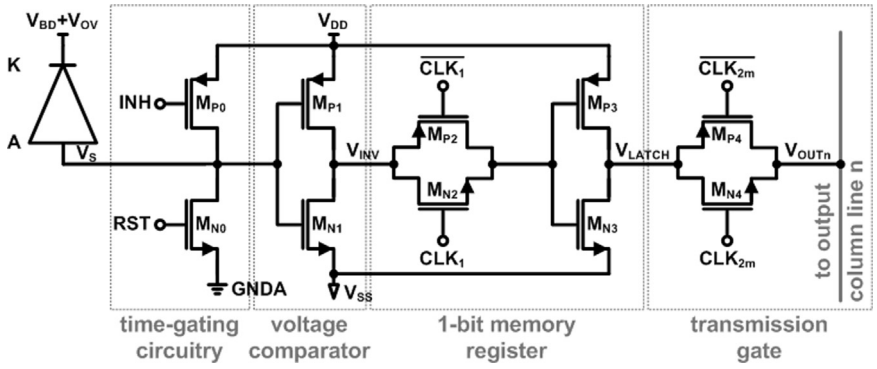

Fig. 1. Schematic diagram of the time-gated digital pixel.