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Monolithic pixels on moderate resistivity substrate and sparsifying readout architecture

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ABSTRACT

The LePix projects aim realizing a new generation monolithic pixel detectors with improved performances at lesser cost with respect to both current state of the art monolithic and hybrid pixel sensors. The detector is built in a 90 nm CMOS process on a substrate of moderate resistivity. This allows charge collection by drift while maintaining the other advantages usually offered by MAPS, like having a single piece detector and using a standard CMOS production line. The collection by drift mechanism, coupled to the low capacitance design of the collecting node made possible by the monolithic approach, provides an excellent signal to noise ratio straight at the pixel cell together with a radiation tolerance far superior to conventional un-depleted MAPS. The excellent signal-to-noise performance is demonstrated by the device ability to separate the 6 keV ^{55}Fe double peak at room temperature.

To achieve high granularity (10–20 μm pitch pixels) over large detector areas maintaining high readout speed, a completely new compressing architecture has been devised. This architecture departs from the mainstream hybrid pixel sparsification approach, which uses in-pixel logic to reduce data, by using topological compression to minimize pixel area and power consumption.

1. Introduction

When in any scientific, technological or commercial applications the position of a particle has to be measured, most of the times pixel detectors are the sensors of choice. In many cases an integrate image of the particle flux is sufficient; in other cases (High Energy Physics, medical imaging, etc.) precise position and timing measurements must be performed on any single incoming particle. In this latter case, together with the spatial resolution and the sensitivity, the other key benchmark is the detector time resolution, i.e. its capacity to separate events in time other than in space. To allow single particle position reconstruction, in fact, in any given frame the number of hits must be as low as it makes it possible to unambiguously distinguish them [7]. In this condition the actual number of pixels carrying useful information in any given frame (occupancy) is quite low, usually in the order of few per cent of the total at maximum. To maximize the frame rate data compression is thereby mandatory. In many practical cases the integrate image case can be derived by digital integration of the recorded cluster positions, with the potential benefit of higher spatial resolution in the latter case [7].

The LePix project targets these high speed particle tracking applications, like those found in High Energy Physics (HEP). The HEP community faced the challenge of particles tracking at the LHC experiments, where high speed (40 MFrames/s), granularity (100 μm pixels) and extreme radiation tolerance (10^{15} neutrons/cm^2) were paramount [3]. Special pixel detectors have been developed during the last decade mostly inside the HEP community to address the challenge of particle tracking at LHC experiments. The specific requirements for speed, spatial resolution and radiation hardness, among others, lead to a common solution adopted in different flavors by all the major experiments, the so-called hybrid pixel detector. In a hybrid pixel detector the sensitive pixel matrix is built using a specifically tailored material coupled to a matching readout matrix realized in a commercially available

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IC technology. The obvious advantage of such a solution is the possibility of optimizing the sensitive material, avoiding the technological constraints inherent to the readout electronic layer fabrication process. To maximize charge collection a bias is usually applied to deplete the sensitive volume: charge carrier pairs do not recombine and the charge is collected by drift, extending the collection range to the whole depleted volume. Response speed also improves, as collection by drift is much faster than collection by diffusion. Radiation tolerance improves as well (up to 10^{15} n/cm^2 in present devices), as charge carriers are less prone to get trapped by the lattice defects caused by the radiation. The basic drawback of such an approach is the inherent complexity of assembling the sensitive and the readout layers. The bump-bonding process, where small (down to 20–50 μm) metal balls connect the matching pads present on the detector and the readout dies, is complex, time-consuming and costly. Furthermore, even the most recent technologies cannot provide a pitch finer than 30–50 μm. The parasitic capacitance introduced by the ball connection also limits the maximum signal to noise ratio, adversely affecting the analog power consumption.

Differently from hybrid detectors, monolithic pixel detectors integrate sensor and readout in one piece of silicon, therefore favorably comparing in terms of assembly, production cost and simplicity [1]. Lacking the parasitic capacitance introduced by the connection between the detector and the collection node, monolithic devices exhibit very low detector capacitance (on the order of some fF), allowing for low power operation. In traditional monolithic detectors charge is collected by diffusion, which means an intrinsic low signal (collection range of ~10 μm) and low resistance to radiation damage, one of the main reasons they have not yet been widely adopted for HEP. Charge collection by diffusion was a mandatory choice as the substrate (the silicon support the active electronic layer is built upon) is usually made by very low resistivity silicon, which makes it unsuitable for depletion. Further limitations arise from the fact that the electronics share the space with the collection node inside the pixel. Therefore the number of transistors must be limited, to avoid a rise in the detector capacitance, and their type can be limited, depending on the technology, to avoid their body from subtracting signal charge to the collection node [6]. Anyway, most recent MAPS processes started to be available with high-resistivity epitaxial layers or high-resistivity substrates, like LePix. Most recent results from high-resistivity epitaxial layer monolithic pixels demonstrate how such technology can improve MAPS radiation tolerance and general performances level of more than one order of magnitude [4], leading to radiation tolerance in excess of 10^{13} neutrons/cm^2.

The LePix detector joins this trend, taking the monolithic technology to a performance level comparable, and even superior in many aspects, to the hybrid pixel one, maintaining at the same time the production, assembly and cost advantages characteristics of the monolithic approach.

2. Detector design

Two mechanisms exist to collect charge generated in silicon by ionizing radiation: diffusion and drift. In the case of diffusion there is no strong force acting on the charge carriers: they undergo random-walk, and those which do not recombine or get trapped ultimately get collected on a charge collection electrode. The process is slow (some hundreds of ns), increasing the chance for the charge carriers to be captured by defects or traps in the material. Charge collection by diffusion is used in traditional monolithic pixel detectors, where radiation tolerance therefore does not exceed fluences of 10^{12}–10^{13} neutrons/cm^2, often already with significant performance degradation at lower fluences. Charge collection is limited to a 10–15 μm epitaxial layer into the material, therefore limiting signal size, yielding signal-to-noise ratios for minimum ionizing particles of only a few tens despite the very small collection electrode capacitance of a few fF.

In contrast silicon detectors traditionally used in HEP collect signal charge primarily by drift. They show tolerance to fluences of 10^{15} neutrons/cm^2 and collect charge over a depth of several hundred microns in a few nanoseconds. To achieve this, an electric field and hence depletion is needed over this depth requiring a high resistivity substrate. The higher the resistivity, the easier the depletion and the charge collection over a certain depth will be achieved. Apart from signal size, timing and radiation tolerance, an often neglected difference is the larger cluster size in case of charge collection by diffusion. Cluster size has a very significant effect on device performance and data reduction effectiveness: dividing the charge over more than a few pixels reduces the effective signal-to-noise and all parameters depending on it, like for instance position resolution. Furthermore, the necessity to transmit more pixels for every cluster requires an increased bandwidth.

The LePix detector is a monolithic pixel detector built with 90 nm IBM CMOS process over a mid-resistive substrate. By depleting the substrate with reasonably low voltages (less than 100 V) it is possible to implement the charge collection by drift is hence achieved within a monolithic detector. Charge collection by drift requires a substrate of sufficiently high resistivity, the higher the better. IBM offers substrates above 500 Ω cm on all their CMOS technologies, even including the very advanced ones processed on 300 mm wafers. This is important for a number of reasons: first, a doping level within one order of magnitude of that of traditional detectors allows charge collection by drift with very low bias voltages. Second, advanced technologies (90 nm or better) will be needed for high speed data transmission and to reduce the dead areas at the detector periphery due to the ancillary circuits, thus facilitating the tiling of the detectors to cover large areas uniformly. Third, wafer size will be crucial to manufacture large modules by stitching. For the LePix detector development the 90 nm CMOS process has been chosen, as it is the first technology offered with low-k dielectrics in the metal stack, so that even with high metal density the parasitics remain limited.

The detector matrix is formed by a two-dimensional array of N-well diffusions into a P-type substrate of moderate resistivity (500 Ω cm). Each of these N-well diffusions create the detecting diode for one pixel. The N-well diffusion forms the charge collection electrode, and contains the local readout circuit for the pixel. The local readout circuit is connected to the periphery where the remainder of the readout circuit is located in an N-well. The NMOS transistors are systematically placed in a P-well inside the N-well (use of triple well technology). Charge collection electrodes and readout circuit are biased near ground (a power supply of $\sim$1 V) with the P-type substrate negatively biased to several volts. To sustain the reverse substrate voltage, readout circuit and detector matrix are surrounded by a guard ring structure. By applying a sufficient reverse substrate bias a bath-tub shaped depletion layer forms underneath the detector matrix, ending near the outer edge of the guard ring. The substrate bias is applied through a top side contact placed outside the guard ring area. The actual detector is a 32×32 pixels matrix of 50 μm pixel pitch. The matrix columns are further divided into four different groups of 8×32 pixels, each sector implementing a different input device. Sectors 1 and 2 both use thin oxide PMOS transistors, smaller in the first and bigger in the second. Sector 3 implements a thick oxide PMOS transistor and sector 4 an NMOS one (Fig. 1). The thin oxide transistors exhibit more gate leakage, which is not an issue in the thick oxide PMOS. The NMOS input device does not exhibit this problem, at the price of a much larger parasitic

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