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Planar pixel detector module development for the HL-LHC ATLAS pixel system ☆

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ABSTRACT

The ATLAS pixel detector for the HL-LHC requires the development of large area pixel modules that can withstand doses up to 10^{16} 1 MeV n_{eq} cm^{-2}. The area of the pixel detector system will be over 5 m^2 and as such low cost, large area modules are required. The development of a quad module based on 4 FE-I4 readout integrated chips (ROIC) will be discussed. The FE-I4 ROIC is a large area chip and the yield of the flip-chip process to form an assembly is discussed for single chip assemblies. The readout of the quad module for laboratory tests will be reported.

1. Introduction

The Large Hadron Collider (LHC) at CERN is the world's highest energy particle accelerator. At present it collides two proton beams each with a centre of mass energy of 7 TeV. One of the four large experiments on the LHC is the general purpose ATLAS [1] experiment. The tracking detector of the ATLAS experiment consists of, going from the vertex out to larger radius, a silicon pixel based system [2], a silicon microstrip based system (SCT) and finally a transition radiation tracker (TRT).

To realise the full physics potential of the LHC a series of luminosity upgrades are planned to the accelerator, resulting in the High-luminosity LHC (HL-LHC) [3,4]. The HL-LHC will have an order of magnitude increase in instantaneous and integrated luminosity over the LHC, from a few 100 fb^{-1} to 3000 fb^{-1} in 10–12 years of planned operation. To cope with the associated increase in event multiplicity and radiation damage the ATLAS experiment will also undergo a series of upgrades.

The increased occupancy, due to the high number of pile-up events per bunch crossing, necessitates a complete replacement of the ATLAS inner detector with a higher granularity system. The tracking system will be a full silicon system with, in the barrel region, 5 layers of silicon strip detectors extending from a radius of about 30 cm from the interaction point. Due to occupancy considerations, the strip length is divided into long (≈5 cm long, in the outer three layers) and short (≈2.5 cm long, for the inner two layers) strips. The four layer pixel detector system (with layers at radii of 39, 75, 160, and 250 mm) is located inside the strip system where occupancy and radiation damage become too large for strip detectors.

The expected maximum fluence will ultimately increase to a maximum level, at the innermost layer, of 2×10^{16} cm^{-2} 1 MeV equivalent neutrons (1 MeV n_{eq}) [5], consisting essentially of charged particles. The level falls to 10^{15} cm^{-2} 1 MeV n_{eq} at the outermost pixel layer. Such doses are unprecedented for silicon detectors and work on the design of detector systems that yield sufficient signal to noise performance are under way. The leading sensor technology under investigation, presented here and elsewhere in this proceedings [6], is the planar silicon sensor with a p-type bulk and n-type segmented implants. The sensor technology for the inner most radius is still more open for investigation with 3D silicon and diamond sensors, as well as planar silicon, also being investigated.

Due to the large size of the pixel system, large area pixel modules are being investigated. The development work uses the FE-I4 [7] chip that has been developed for the ATLAS inner B-layer upgrade (IBL) [8]. The FE-I4 ROIC is produced in 130 nm CMOS technology, which allows for a smaller pixel size, increased in-pixel processing power and reduced power dissipation compared to the present ATLAS pixel ROIC the FE-I3 [9]. For zero pixel occupancy the FE-I4 draws 675 mW, (195 mW cm^{-2}), compared to the FE-I3 which draws 220 mW (380 mW cm^{-2}). The individual pixel size is reduced from the present 50×400 μm^2 to 50×250 μm^2 to cope with the increase in hit occupancy. The 50 μm dimension has been kept to allow the flip-chip processing to take place.

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The FE-I4 is the largest ROIC produced for particle physics applications and is nearly six times larger in area that the present FE-I3 ROIC (3.36 cm^2 compared to 0.58 cm^2 of active area). The proposed pixel system will use modules that consist of 2×2 FE-I4 ROICs, (known as a quad module). The pixel modules aim to have a high active area (≈90%), which is achieved through the use of a large area ROIC with minimised dead space due to periphery pixel chip logic and control circuits. To reduce mass the ROIC will be thinned to 150 μm or less. The sensor will also be 150 μm thick, which has the additional benefit of reduced sensor power load, as well as mass reduction. The data from the 4 FE-I4 ROICs on a module will be multiplexed together to reduce the material due to the signal lines. The system will use serial powering to reduce the amount of material in the services; via less material in the power cable and in the cooling system.

The paper presents work on the design of silicon sensors produced at Micron Semiconductor Ltd,[1] the yield of thin ROICs flip-chip bonded at VTT[2] to these sensors, and the first results from a quad module.

2. Sensors

Two sensor wafer designs that are compatible with the FE-I4 ROIC have been produced at Micron Semiconductor Ltd. They have been fabricated on 6 in. 10 kΩ cm p-type float zone silicon wafers. The segmented side is a heavily doped n-type implant with a p-spray isolation between them. Wafers of 300 μm and 150 μm in thickness have been produced. Results only from the 300 μm devices are shown here. These devices show a full depletion voltage, before irradiation, of 70 V, as expected from their resistivity.

The first of the two wafers, known as CERN Pixel II, has pixel sensor arrays compatible to the FE-I4 readout chip. There are 14 single and 5 two chip FE-I4 sensor designs. The two chip design has a guard structure around the pixel array that matches two FE-I4 chips. The inter-chip region is filled with active silicon. This is achieved with the use of an implant on the last column of one chip and the first of the next of 450 μm in length rather than 250 μm. The single sensors include three different guard ring structures. Two designs have 8 guard rings that are 390 μm wide in total, while the third set has only 4 guard rings with a total width of only 200 μm. This design is known as the slim edge sensor. Sensors with reduced dead space at the edge are attractive for building particle physics experiments as it allows the close packing of the modules on a stave. This removes the requirement to shingle modules on two surfaces of a stave structure, resulting in a lower mass, easier to build system. Such an assembly approach has been required by the ATLAS IBL due to space limitations. For the full HL-LHC upgrade a similar approach is also desired.

The second wafer, known as CERN Pixel IV, has 5 quad sensors and 8 single chip FE-I4 designs. One of the quad sensors includes a slim edge design. The quads have been designed with the inter-chip region filled with active silicon. This is achieved with the use of an implant on the last column of one chip and the first of the next of 450 μm in length rather than 250 μm, as with the two chip sensor design. The separation between the two chips in the row direction is either 850 μm or 450 μm. The area remains active with the use of eight or four extra pixel implants per ROIC. These are attached one each to the outer four pixels, and as such, are connected to the ROIC. When these are hit there is a two pixel ambiguity which needs to be resolved with the use of the tracking system. The design of top metal layer of the pixel sensor is shown in Fig. 1 for the area where the four FE-I4 ROICs are bonded for the design with four extra pixel implants between each ROIC.

Two of the single chip sensors on this wafer have an implant that is 25×500 μm^2 in size rather than the 50×500 μm^2 of the read-out cell. This is achieved with the pixel bump pads being in the same position as the standard sensor, and therefore maintains compatibility with the FE-I4 ROIC. Such a design will enable increased r–Φ resolution in the detector for the same pixel area, but with a reduced resolution in the z-direction.

The single chip sensors current-voltage characteristics showed a current of approximately 10 nA at a reverse bias voltage of 90 V, which is above full depletion. This corresponds to a current density of better than 3 nA cm^{-2} measured at a temperature of 20 °C. The breakdown voltage of the device was design dependent. The best devices were able to hold 1000 V, while the more typical value was 400 V. The slim edge devices typically showed a dramatic increase in current at 150 V, which is to be expected in a non-irradiated device as with bias the depletion region extends laterally to the cut edge.

Building on the success of the two CERN Pixel wafer designs a new sensor wafer is under development. One of its aims is to investigate sensors that are compatible with the FE-I4 ROIC that have alternative implant structures, for example square pixels. Such a pixel structure might lead to benefits in the forward, high pseudo-rapidity region of the detector system, covered by the pixel disk system.

3. Single chip assemblies

Four sensor wafers, two of each design, and three FE-I4 ROIC wafers were shipped to VTT for under-bump metal deposition (UBM), lead-tin solder ball deposition and flip-chip assembly. Both the sensor and ROIC wafers had the UBM deposited upon them. Only the ROIC had the PbSn electroplated and reflowed to form solder bumps. After solder bump deposition one of the two ROIC wafers was back thinned to a thickness of 200 μm. This represented the first stage at making assemblies with thin ROICs required for the ATLAS HL-LHC pixel system. The ROIC wafers were diced and the bumps visually inspected for missing or shorted bumps. The yield of the bump deposition and re-flow process was high with only 12% of the ROICs being rejected due to poor bump yield; defined as more than 25 faulty bumps in the matrix of 26880 bumps, corresponding to 0.1%.

The ROICs were flip-chipped to the sensors with an FC-150 SET machine at VTT. A weak tack bond was made on the machine. The assemblies were then transferred to a re-flow oven, with a reducing atmosphere, to reflow the solder bumps at 260 °C. The sensor and ROIC were held on SiC vacuum jigs on the FC-150 machine. However, in the re-flow oven they are not held flat under vacuum and could therefore bow.

Fifteen single chip assemblies have been produced all with ROICs from the 200 μm thick wafer. Of these, 5 assemblies have been mounted onto test cards and tested in the laboratory and at test-beams. The other 10 devices have not been mounted and will be sent for irradiation to prove the radiation hardness of the assemblies.

The sensor wafers were all probed after fabrication while on the wafer, after UBM deposition and wafer dicing and after assembly into a module. The current-voltage characteristics of the sensors did not change relative to the initial measurements, except that a few showed a slightly improved high voltage characteristic, as illustrated in Fig. 2.

The tested devices have been characterised with the use of the USBPix test system [10] in the laboratory at a temperature of 20 °C and at test-beam (not reported here). The goal of the laboratory characterisation was to prove the yield of the flip-chip process and the noise performance of the modules. The initial characterisation stage required the tuning of the DACs that control the in-pixel

[1] Micron Semiconductor Ltd. www.micronsemiconductor.co.uk.
[2] VTT Technical Research Centre of Finland, http://www.vtt.fi.