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A fast hardware tracker for the ATLAS trigger system

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ABSTRACT

The fast tracker (FTK) is an integral part of the trigger upgrade program for the ATLAS detector at the Large Hadron Collider (LHC). As the LHC luminosity approaches its design level of 10^{34} cm^{-2} s^{-1}, the combinatorial problem posed by charged particle tracking becomes increasingly difficult due to the swelling of multiple interactions per bunch crossing (pile-up). The FTK is a highly-parallel hardware system intended to provide high-quality tracks with transverse momentum above 1 GeV/c. The FTK systems design, based on a mixture of advanced technologies, and expected physics performance will be presented.

1. Introduction

Selecting interesting events online is a very challenging task in the Large Hadron Collider (LHC) experiments. By the end of 2014, the LHC will run with an energy of 13 or 14 TeV and instantaneous luminosities which could exceed 10^{34} interactions per cm^2 and per second. The triggering in the ATLAS detector [1] is realized using a three-level trigger approach, in which the first level is hardware based and the second and third stages are realized using large computing farms. It is a crucial and non-trivial task for triggering to maintain a high efficiency for events of interest while suppressing effectively the very high rates of inclusive QCD processes, which constitute mainly background. At the same time the trigger system has to be robust and provide sufficient operational margins to adapt to changes in the running environment. In the current design track reconstruction can be performed only in limited regions of interest at second trigger stage and the CPU requirements may limit this even further at the highest instantaneous luminosities. Providing high quality track reconstruction over the entire detector volume for the second stage trigger decision would allow gains in efficiency and background rejection for triggers on tau leptons and b-hadrons and help to improve the performance decrement of isolation by the luminosity increasing for electrons and muons. The fast track trigger (FTK) [2] is an ongoing upgrade project aimed at providing real time track for the trigger using the silicon microstrip and pixel detectors. Pattern recognition and track fitting are executed in a hardware system utilizing massive parallel processing and achieve a tracking performance close to that of the global track reconstruction. Its speed and physics performance have been estimated at simulated luminosities up to 3×10^{34} cm^{-2} s^{-1}, corresponding to 75 interactions per bunch crossing.

2. The ATLAS detector and trigger

ATLAS is one of the general-purpose detectors at the LHC. It is designed to detect the products of proton–proton collisions at a center of mass energy of 14 TeV. Particles are detected by the inner tracking detector, electromagnetic and hadronic calorimeters and the muon system. The inner tracker is inside a 2-T solenoidal magnetic field. The FTK will use information from the pixel and strip inner silicon tracker systems shown in Fig. 1. To select interesting physics events created by multiple p–p collisions at 40 MHz frequency, a three-level trigger system is used [3]. The Level-1 trigger is hardware-based and has a maximum output rate of 100 kHz. It provides regions of interest to the next two levels. Level-2 and the event filter are implemented in software and are collectively known as the high level trigger (HLT). The HLT runs on a farm of several thousand CPUs. Level-2 operates within regions of interest with an output rate of about 6 kHz, while the event filter has access to all information in the event, with an output rate of about 400 Hz.

3. FTK system

The FTK will operate at full Level-1 output rates, providing high-quality tracks reconstructed in the entire inner detector by the start of processing in the Level-2 trigger. The execution time in

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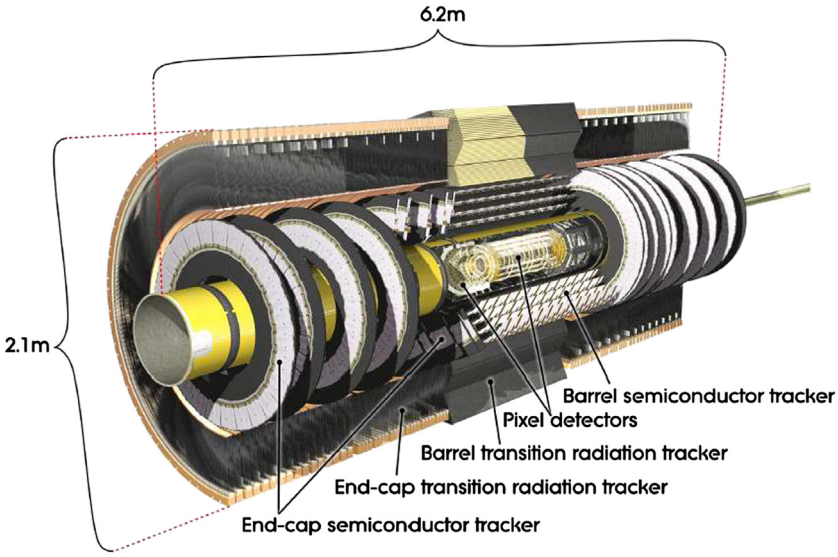

Fig. 1. Cut-away view of the ATLAS inner detector.

the Level-2 farm for more complex selection algorithms is allowing more interesting events to be selected with higher efficiency. FTK solves the combinatorial challenge inherent to tracking by exploiting the massive parallelism of associative memories that compare inner detector hits to billions of precalculated patterns simultaneously.

The tracking on the matched patterns, referred to roads, is further simplified by transforming the helix parameters (P_T, η, ϕ, d_0, z_0) and the quality estimator calculations into a set of scalar products in the form

$$p_i = \sum_j C_{i,j} x_j + q_i$$

where x_j are the hit coordinates in each detector layer, $C_{i,j}$ and q_i are precalculated terms, and p_i is either a helix parameter or a χ^2 quality estimator. This transformation that implemented in modern commercial programmable gate arrays (FPGA) can perform the calculation in a very efficient and parallel way.

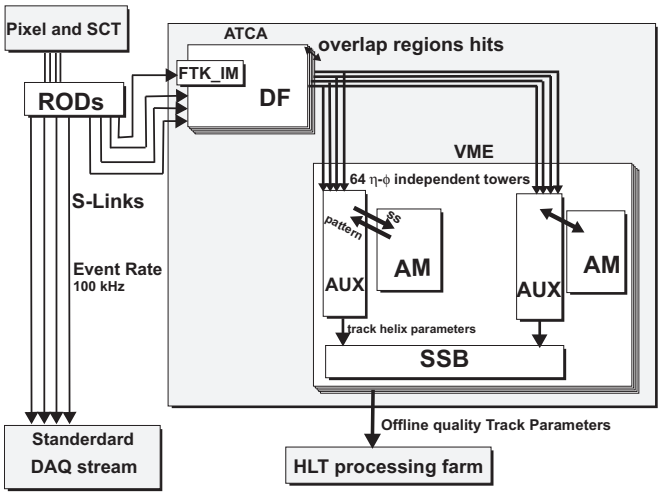

Fig. 2. FTK architecture.

4. FTK architecture

The FTK system will receive a copy of the data from the ATLAS pixel and strip detectors. The extra capability of sending a second copy of the data from detector was not present in the original high-speed optical link for ATLAS (HOLA) card, responsible for the output. Therefore, a specific dual-output HOLA card was developed for the FTK: it has two independent streams, one for the standard data acquisition (DAQ) stream and the second for FTK. A total of 270 dual-output HOLA cards are required to serve the FTK, which all have been produced and tested. The testing procedure was particularly detailed and important because these cards are used by the general DAQ; indeed a failure would prevent normal ATLAS operations. During the 2011–2012 winter shutdown 32 dual-output HOLA cards were installed and included in normal ATLAS data-taking operations since then.

The data sent by the HOLAs to the FTK will be collected by the data formatter (DF). The DF organizes the data to be used by the FTK system. It maps the silicon inner detector (ID) modules to 64η–ϕ independent towers (16 in ϕ, 4 in η). The DF sends hits of 8 out of 11 layers to the associative memory (AM) chip. The data from the other three layers are sent to the second stage boards (SSB). In the AM, data from eight layers are used for pattern recognition, and the remaining three layers are used to remove fakes. Technically, the DF boards will be installed in advanced telecommunications computing architecture (ATCA) crates [4]. This architecture was chosen because of the data sharing flexibility in ATCA. The AM boards will be installed in VME crates. For the communication of each DF crates, and connection between DF and AM, an optical fiber will be used.

A special role is played by the input mezzanine card installed in the DF boards, which is called the FTK_IM. This mezzanine card receives inputs from the fibers connected to the HOLA cards and runs a clustering algorithm. The clustering algorithm is crucial in the pixel layer to identify the pixel hit clusters and calculate the centroids. The data from strip detectors are already clustered with the maximum cluster width of two by the front-end chip, and for instrumental reasons clusters can be split at chip boundaries.

The data collected by the DF will be sent to the processing units, composed by the AM board and an auxiliary card (AUX) installed on the VME back-plane. Technically the AUX card receives the full resolution hits and converts them to coarser resolution hits, called super strip (SS), to make pattern recognition more efficient and speedy. The SS information is routed within the AM board to 128 AMChip04 chips [5] and matched to patterns, about