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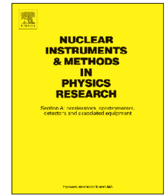

Characterization of SOI monolithic detector system

P.L. Álvarez-Rengifo [a,b,*], L. Soung Yee [a], E. Martin [b], E. Cortina [a], C. Ferrer [b]

[a] Université catholique de Louvain, Louvain-la-Neuve, Belgium
[b] Universitat Autònoma de Barcelona, Barcelona, Spain

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ABSTRACT

A monolithic active pixel sensor for charged particle tracking was developed. This research is performed within the framework of an R&D project called TRAPPISTe (Tracking Particles for Physics Instrumentation in SOI Technology) whose aim is to evaluate the feasibility of developing a Monolithic Active Pixel Sensor (MAPS) with Silicon-on-Insulator (SOI) technology. Two chips were fabricated: TRAPPISTe-1 and TRAPPISTe-2. TRAPPISTe-1 was produced at the WINFAB facility at the Université catholique de Louvain (UCL), Belgium, in a 2 μm fully depleted (FD-SOI) CMOS process. TRAPPISTe-2 was fabricated with the LAPIS 0.2 μm FD-SOI CMOS process. The electrical characterization on single transistor test structures and of the electronic readout for the TRAPPISTe series of monolithic pixel detectors was carried out. The behavior of the prototypes' electronics as a function of the back voltage was studied. Results showed that both readout circuits exhibited sensitivity to the back voltage. Despite this unwanted secondary effect, the responses of TRAPPISTe-2 amplifiers can be improved by a variation in the circuit parameters.

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1. Introduction

Hybrid detectors, in which the sensor and the electronics are built separately and then bonded together, are admirably performing with the very high speed used at the readout ASIC. These detectors have, nonetheless, some limitations in current particle physics applications due to the two separate layers [1]. Particularly, because of the demands on high resolution in high-multiplicity environments (i.e. small cell size), radiation hardness, and material budget. This problematic integration step has led to increased efforts related to monolithic solutions in which the sensor, the amplification, and the logic circuitry are found in the same silicon wafer.

The SOI technology presents the possibility of developing monolithic radiation detectors. A detector implant is made in the bottom handle wafer and connected to readout electronics in the top active layer. The two parts are insulated from each other by a buried oxide layer. This decreases parasitic capacitances and allows a more compact layout (see Fig. 1).

Using this approach, a high resistivity silicon handle wafer can be employed to build the sensor while using lower resistivity silicon for the electronic devices. However, the close proximity of the parts can result in undesirable interference between the detector and the electronics. Besides, a backgate effect occurs when the substrate bias voltage that depletes the detector, back voltage (V_{BACK}). Fig. 1 shows the monolithic pixel developed in a SOI wafer. The P_{+} bias ring is used to bias the detector in the handle wafer. It is nominally grounded and a voltage applied to the back contact of the chip, (V_{BACK}), is used to deplete the pixel sensor. In addition, the N_{+} substrate contact ring provides a direct contact to the handle wafer and may be used to deplete the detector area from top side of the chip with voltage V_{DET}. Herein, V_{BACK} was used to deplete the detector. Since the area under the transistor acts as a back gate, its potential affects the threshold voltage and the leakage current of the transistor. These effects need to be studied before implementing the SOI technology. One of the main goals of the TRAPPISTe (Tracking Particles for Physics Instrumentation in SOI Technology) project is to analyze the above mentioned effects and to try to minimize them. In this work, two SOI technologies were used and two different readout approaches were evaluated.

2. TRAPPISTe SOI technology

A first prototype (TRAPPISTe-1) was developed at the Université catholique de Louvain (UCL) in Belgium at the WINFAB facility in Louvain-la-Neuve. WINFAB provided a 2 μm FD-SOI CMOS process [2]. For this prototype, a larger feature technology with thicker layer thicknesses and a p-type wafer with a low resistivity of about 25 Ω cm was used. A low resistivity handle wafer is not ideal for detector development as higher back voltages are required to deplete the detector. However, the first prototype was fabricated using a low resistivity wafer due to wafer availability. The TRAPPISTe-1 prototype is an 8 × 8 pixel matrix with a

* Corresponding author. Tel.: +32 10 47 3227.
E-mail address: paula.alvarez@uclouvain.be (P.L. Álvarez-Rengifo).

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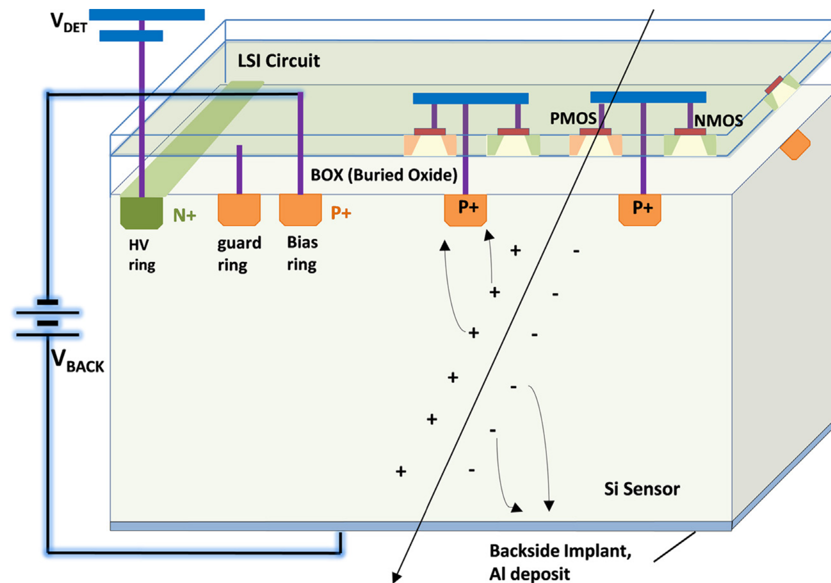

Fig. 1. Sketch of a monolithic pixel developed in a SOI wafer.

shift register used to control signal readout. Each pixel contains a 3-Transistor (3T) readout and has dimensions of 300 μm × 300 μm [3]. As a separate study, an additional set of charge sensitive amplifiers (CSA) was produced on another run using the same technology. This additional design was used to validate the architecture with SOI, although no connection with the detector was included [4].

A second prototype, TRAPPISTe-2, was fabricated with a 0.2 μm FD-SOI CMOS technology, provided by LAPIS Semiconductors through the SOIPIX collaboration [5]. The LAPIS process provided high resistivity n-type substrates of 700 Ω cm and 10 kΩ cm. Besides, the smaller feature size and higher number of metal layers allow for higher integration of circuitry. The two different technology processes are summarized in Table 1.

The second phase of this project was developed with the TRAPPISTe-2 prototype, see Fig. 2. This version included similar readout architectures for evaluation and several test transistors. The architectures were the basic 3-transistor readout and a charge sensitive amplifier with a shaping amplifier. The smaller feature size of the LAPIS technology allowed smaller pixel sizes (150 μm × 150 μm), as well as the integration of the charge sensitive amplifier inside a pixel. The matrix implemented was the 6 × 6 pixels.

In both developments, the backgate effect was evaluated. The first WINFAB technology uses a 400 nm thick buried oxide layer [2]. The LAPIS technology provides a method to mitigate the backgate effect with a buried P-well (BPW). The first results to be presented are based on measurements performed at different back voltages. The voltage applied to the detector in the handle wafer can alter the operation of the circuitry in the top layer above.

Table 1
Summary of TRAPPISTE process technology properties.

Technology properties	WINFAB	LAPIS
Process	2 μm FD-SOI	0.2 μm FD-SOI
Top active layer	100 nm	50 nm
Buried oxide layer	400 nm	200 nm
Bottom handle layer	≈500 μm	≈300 μm
Handle layer type	p-Type	n-Type
Handle layer resistivity	15–25 Ω cm	10 kΩ cm
Metal layers	1	5
Polysilicon layers	1	1

3. Transistor characterization of TRAPPISTe-2

A validation of our transistors at different back voltage was performed first. For the characterization, results from measurements carried out on the TRAPPISTe-2 test structures are presented. The transistor test area contains single devices whose gate, source, and drain inputs are connected to test pads. It contains seven columns of transistors representing the source tied transistors provided by the LAPIS process. All of the transistors have a W/L of 10 μ/2 μ except for the I/O n-type Depleted MOS (DMOS) transistors which are 2 μ/10 μ in size.

Parameters such as the threshold voltage (V_{th}), the mobility (μ_0), and the transconductance (g_m) were characterized. The method used to characterize the transistors was based on the linear-extrapolation technique in which V_{th} is obtained by the linear extrapolation of the $F_1(V_G)=I_d/\sqrt{g_m}$ (V_{th1} in Fig. 3). Another additional method, based on the calculation derivate where $F_2(V_G)=\sqrt{[3]A}/2(V_G-V_{th})$ and $A=\mu_0 C_{ox} V_D W/L_{eff}$, was used to validate the obtained results (V_{th2} in Fig. 3) [6].

The above measurements were performed at different back voltages. The extraction of parameters is an important part of the device modeling and of the characterization process. The obtained parameters can be seen in Fig. 3 for NMOS with low and standard threshold voltages. For these calculations, two conditions of drain voltage (V_d) were used: 20 mV and 50 mV. The threshold voltage decreased with the increasing of V_{BACK}. Consequently, as shown in Fig. 3, an increase of V_{BACK} greater than 10 V generated a condition in which an optimal performance of the transistors is not possible.

4. Charge sensitive amplifier measurements

Charge sensitive amplifiers were implemented in both WINFAB and LAPIS technologies. Amplifiers were based on a standard folded cascode core with a feedback capacitor (see Fig. 4). The CSA converts

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