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Measurement results of DIPIX pixel sensor developed in SOI technology

Mohammed Imran Ahmed [a,b,*], Yasuo Arai [c], Marek Idzik [a], Piotr Kapusta [b], Toshinobu Miyoshi [c], Michal Turala [b]

[a] AGH University of Science and Technology, Faculty of Physics and Applied Computer Science, Krakow, Poland
[b] Institute of Nuclear Physics Polish Academy of Sciences, Krakow, Poland
[c] Institute of Particle and Nuclear Studies, High Energy Accelerator Research Organization(KEK), Tsukuba 305-0801, Japan

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ABSTRACT

The development of integration type pixel detectors presents interest for physics communities because it brings optimization of design, simplicity of production—which means smaller cost, and reduction of detector material budget. During the last decade a lot of research and development activities took place in the field of CMOS Silicon-On-Insulator (SOI) technology resulting in improvement in wafer size, wafer resistivity and MIM capacitance. Several ideas have been tested successfully and are gradually entering into the application phase. Some of the novel concepts exploring SOI technology are pursued at KEK; several prototypes of dual mode integration type pixel (DIPIX) have been recently produced and described. This report presents initial test results of some of the prototypes including tests obtained with the infrared laser beams and Americium (Am-241) source. The Equivalent Noise Charge (ENC) of 86 e^- has been measured. The measured performance demonstrates that SOI technology is a feasible choice for future applications.

1. Introduction

The trend of bulk CMOS technology makes conventional scaling less feasible, while the demand for high speed and low power large scale integration (LSI) circuit is continuously increasing [1]. After incubated for more than 20 years, the silicon-on-insulator (SOI) CMOS technology is a promising candidate to overcome this fundamental limit of scaling [2]. The additional features of SOI technology are good radiation hardness [3], and ability to handle high voltages and temperatures. Profiting from the insulator buried oxide layer (BOX) separating devices from the substrate, one can select the substrate of required properties, which reveals that SOI is an ideal choice for realizing monolithic pixel detector. The presence of back gate effect which causes a shift in transistor threshold limits the application of large bias voltage making the detector only partially depleted. This effect can be mitigated by implanting lightly doped buried p-type just below the BOX layer. A study performed using technology computer-aided design (TCAD) simulation confirm the functionality of the applied technique [4]. The dual mode integration type pixel (DIPIX) chip was designed at KEK and fabricated in the Lapis Semiconductor Co., Ltd. (previous name OKI Semiconductor) 0.20 μm CMOS fully depleted (FD) SOI process. It has improved wafer size, wafer resistivity and metal–insulator –metal (MIM) capacitance. Several ideas have been developed and tested successfully [5,6] and some of the novel concepts exploring SOI technology are pursued at KEK which includes integration type pixel (INTPIX) and counting type pixel detectors [7]. The DIPIX detector resembles INTPIX with some additional features. This report presents the initial test results of DIPIX detector .

2. Design prototype

The DIPIX1 and DIPIX2 chips include $14 \times 14\ \mu m^2$ integration type pixels with correlated double sampling (CDS) circuit. They differ only in sensor layouts. DIPIX is integrated on a 5×5 mm chip and each chip has 256×256 pixels and 128×256 pixels of two types respectively (see Table 1). The schematic of DIPIX is shown in Fig. 1. The circuit is designed to work both in n-type and p-type substrates. An internal 10-bit Wilkinson type ADC is also included in each column of the chip that makes possible the readout in both analog and digital form. All the measurements shown in this report use an external ADC.

In Fig. 1 the schematic of single pixel circuit is shown. The reverse bias voltage is applied to +Vdet or −Vdet and the reset voltage is applied to Vsense node through V_RSTn or V_RSTp depending on the type of substrate. The "no metal" window of the sensor is illuminated using visible laser light and the detected

* Corresponding author at: AGH University of Science and Technology, Faculty of Physics and Applied Computer Science, Krakow, Poland.
E-mail address: imran.ahmed@fis.agh.edu.pl (M.I. Ahmed).

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Table 1
DIPIX family.

Sensor parameters	DIPIX1	DIPIX2	
Wafers-type	CZ-n	CZ-n	FZ-n
Resistivity (kΩ-cm)	0.7	0.7	7
Pixel size (μm)	14	14	
No. of pixels	256 × 256	128 × 256 × 2	
Chip area (mm^2)	5 × 5	5 × 5	
Effective area (mm)	3.584	3.584	
CDS in Pixel	Yes	Yes	

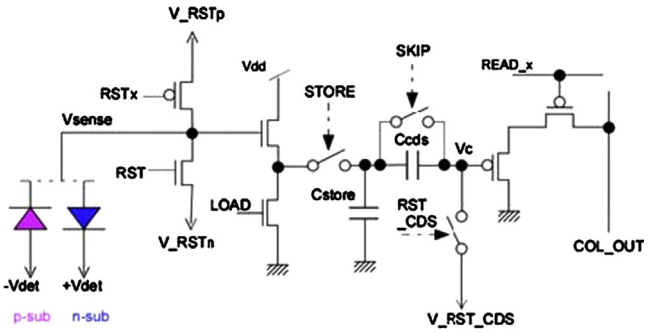

Fig. 1. Schematics of DIPIX1/2 single pixel readout channel.

signal is buffered by the source follower. Two capacitors are used in this circuit, one is a MIM capacitor of 100fF (Cstore) and other is the correlated double sampling (CDS) capacitor of 82fF (Ccds). The signal is stored in the Cstore capactitor. When READ_x is asserted and SKIP switch is closed (Ccds capacitor is short circuit), Vc voltage is readout by an external or internal ADC without CDS. If the SKIP switch is open, the Vc voltage is readout using CDS capacitor. The depletion MOS (DMOS) transistor is used as a CDS capacitor to remove the undesired offset.

3. Measurement and test results

All the measurements shown in this section are done at room temperature i.e. 24 °C with CZ-n (Czochralski n-type) and FZ-n (Float-zone n-type) sensors of DIPIX2 family. The CDS readout is not used in these measurements.

3.1. Stability test

In principle each pixel should be reset after every frame and if there is no signal in the sensor the pixel output should be constant. The stability test is done to check whether the detector is capable of operating in long run measurements. The pixel responses are analyzed in dark without any signal. The behaviour of both sensors are studied as a function of time. The outputs of ADC conversion (average of 10 frames) for two different pixels are plotted over time in Fig. 2. The measurement is taken continuously for 1 h. Systematic changes during first 20,000 frames are due to self-heating and probably may be reduced in future using the CDS.

3.2. Infrared laser test

The response of DIPIX2 has been tested with infrared (IR) laser (PDL 800-D) in pulsed mode with 80 MHz frequency and 1060 nm of wavelength. The 3-dimensional motorized setup (see Fig. 3) is used to focus to a spot size of $\simeq 10\,\mu m$, using the Schfter+Kirchhoff laser optic "60fc-4-a11-02-pq" [8]. Since the spot is smaller than the pixel pitch, the measured signal can

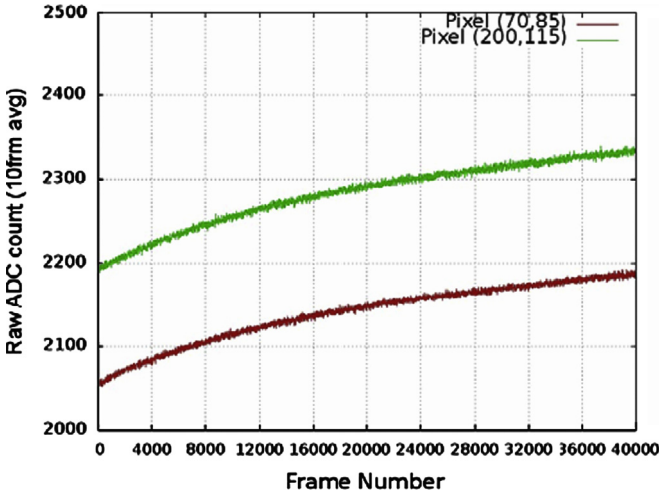

Fig. 2. Stability test of CZ-n by skipping CDS with 40,000 frames for two different pixels (the horizontal scale corresponds to 1 h).

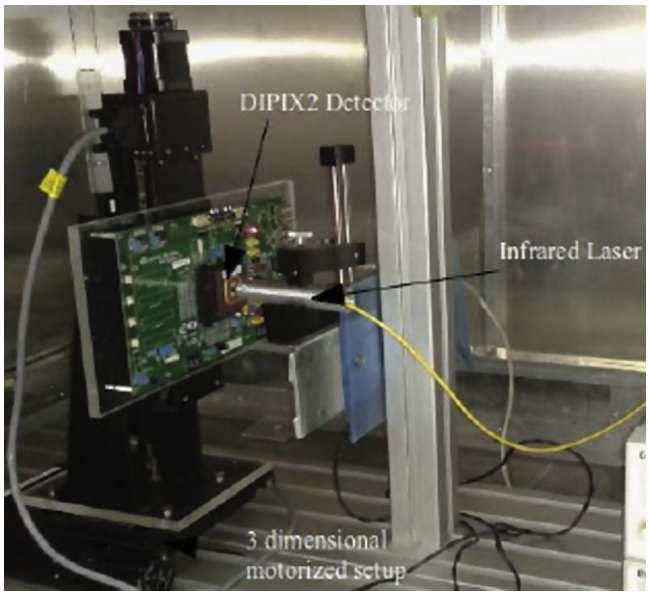

Fig. 3. Laser setup.

be seen mainly in a single pixel. However, we observed a halo effect for very large group of pixels around the illuminated pixel. The amplitudes of these pixels are around 12–15% of the pixel with maximum amplitude and their distribution is beyond the Gaussian. The halo is seen in both sensors and it mostly depends on laser intensity. Fig. 4(a) and (b) shows the result before and after optimizing the laser intensity and back bias voltage for FZ-n sensor. It may be due to large charge generation in a not fully depleted sensor disturbing the electric field. This is confirmed with the Americium data (see Section 3.3). After the scan over laser intensity, integration time and back bias voltage using IR laser, the optimized values are summarized for both sensors (see Table 2). The same conditions were used for Americium (Am-241) measurements.

3.3. Measurements with Americium (Am-241) source

The radioactive source used for this test setup is Am-241 with the activity of 10 mCi (=370 MBq). As the incident photon rate is low (occupancy below 0.1%), we keep the source close to the sensor in the black box. Table 3 gives the radiation information