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LePIX: First results from a novel monolithic pixel sensor

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ABSTRACT

We present a monolithic pixel sensor developed in the framework of the LePIX project aimed at tracking/triggering tasks where high granularity, low power consumption, material budget, radiation hardness and production costs are a concern. The detector is built in a 90 nm CMOS process on a substrate of moderate resistivity. This maintains the advantages usually offered by Monolithic Active Pixel Sensors (MAPS), like a low input capacitance, having a single piece detector and using a standard CMOS production line, but offers charge collection by drift from a depleted region and therefore an excellent signal to noise ratio and a radiation tolerance superior to conventional undepleted MAPS.

Measurement results obtained with the first prototypes from laser, radioactive source and beam test experiments are described. The excellent signal-to-noise performance is demonstrated by the capability of the device to separate the peaks in the spectrum of a ^{55}Fe source. We will also highlight the interaction between pixel cell design and architecture which points toward a very precise direction in the development of such depleted monolithic pixel devices for high energy physics.

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1. Introduction

Monolithic detectors integrate sensor and readout in one piece of silicon and therefore in principle favorably compare with hybrid detectors in terms of detector assembly, production cost and detector capacitance. Despite years of intensive research, however, they have not yet been widely adopted for high energy physics. Some functional devices on high resistivity silicon were developed but often required exotic fabrication steps (e.g. double sided processing [1]), incompatible with high volume manufacturing in standard semiconductor foundries. Recently devices have been manufactured in more standard CMOS technologies, but preserving the low capacitance and efficiency over the full surface for more complex readout circuitry have remained a challenge. This is also the case for Monolithic Active Pixel Sensors (MAPS) [2,3], which typically use a very simple in-pixel circuitry in combination with "rolling shutter" architectures, not always compatible with high-energy physics requirements. These MAPS often collect the signal charge by diffusion over a very limited depth, which makes them very sensitive to radiation damage, results in relatively slow signal collection, and provides only a moderate signal-to-noise ratio despite the low sensor capacitance.

The LePix approach is trying to address these issues by fabricating CMOS on wafers of moderate to high resistivity to obtain a relatively large depletion region (several tens of microns) with a moderate bias voltage (50–100 V) and to collect the signal charge by drift. This results in a large charge signal, minimizes the impact of bulk damage by non-ionizing radiation, helps controlling the charge sharing among different pixels and improves the charge collection speed. The use of non-standard wafers has only a limited impact on the CMOS technology and preserves the possibility of volume manufacturing in a standard foundry.

Analog power is minimized by the large signal collected from the depletion layer and by keeping the sensor capacitance low. The in-pixel circuitry, placed in the N-well collection electrode, is therefore to be kept simple and small. The signal is immediately transferred to the periphery in analog form to save power eliminating the need for clock distribution over the pixel matrix. Hit information is therefore available at the periphery immediately allowing trigger generation. The drawback is the need for a high metal density, since in principle every pixel has to be connected directly to the periphery; this was one of the main

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reasons to choose the 90 nm technology as it offers low-k dielectrics in the metal stack, and therefore high metal pitch with lower parasitics. To take advantage of important power savings in the analog part, also the power in the digital part needs to be reduced significantly. This is further discussed in a later section.

2. Device description

The detector matrix (Fig. 1) is formed by a two-dimensional array of Nwell diffusions into a P-type substrate of moderate resistivity (above 500 Ω cm). Each of these Nwell diffusions creates the detecting diode for one pixel and forms the charge collection electrode. The in-pixel circuitry is placed in this N-well collection electrode, and has therefore to be kept simple and small. The remainder of the readout circuit is located in the periphery, in an Nwell with NMOS transistors systematically placed in a Pwell inside the Nwell (use of triple well technology). Charge collection electrodes and readout circuit are biased near ground (a power supply of ~1 V) with the P-type substrate negatively biased to several tens of volt. To sustain the reverse substrate voltage, readout circuit and detector matrix are surrounded by a guard ring structure. By applying a sufficient reverse substrate bias, a bath-tub shaped depletion layer several tens of micron thick is formed continuous underneath readout and detector matrix and ending near the outer edge of the guard ring. Applying the substrate bias is possible from a top side contact outside the guard ring area.

Charge collection by drift requires a substrate of sufficiently high resistivity, the higher the better. The foundry offered us 90 nm standard CMOS on a substrate with resistivity of several hundred ohms centimeters. This is strategically important since a doping level within one order of magnitude of that of traditional detectors allows depletion layers of ~50 μm or more (see Fig. 3) and therefore large signals. Such an advanced process may not always be needed but it will provide significant benefits in high speed data transmission, pixel detectors for the inner layers, and minimum feature size will also give access to the lowest possible input capacitance and therefore ultimate analog performance.

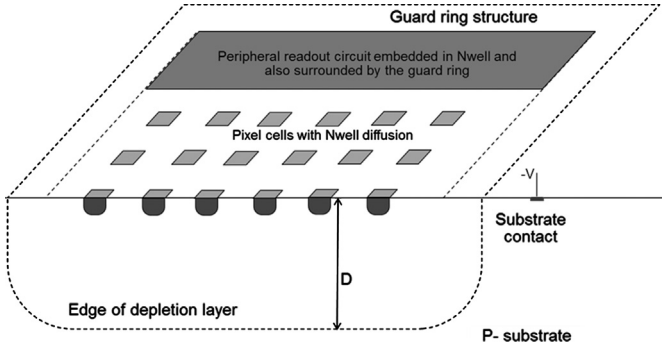

Fig. 1. Schematic detector structure.

The substrate change is in principle a minor process modification, but sustaining significant reverse substrate bias in a 1 V technology and design rules in this advanced process render implementing the detecting diode with a small collection electrode non-trivial in practice: electrostatic discharge protection structures are non-standard as one cannot connect them to the substrate. Density rules of active area and polysilicon enforce patterning of certain regions even if this is not desirable. Creating lowly doped areas to ease depletion is often non-standard and needs special mask generation.

Several prototype chips have been submitted for fabrication: four different pixel matrices, a test structure containing different pixel types, including some that could not be included in the larger matrices, a large diode and a transistor test structure. Two pixel matrices contain an analog integrating readout, and were used to obtain the test results presented here. Two other matrices containing a readout with amplifier, shaper and discriminator (25 ns shaping time) are still under test.

2.1. Readout circuit

Each pixel (Fig. 2) is equipped with a source follower to buffer the signal and drive storage capacitors. Only the PMOS and the reset transistor are in the pixel, current source and storage capacitors are outside of the pixel. The signal timing is as follows: after a reset signal, the analog output of each pixel is stored on a first storage capacitor using a first store command as a reference. The analog output of each pixel is stored a second time to record the collected signal (and possible leakage current) after a second store command. The time lapse between the two store commands determines the integration period during which signal is collected. Thereafter a sequential readout is initiated to read all stored values (2 per pixel). This scheme allows double correlated sampling with full decoupling of integration and readout time, necessary since no data on leakage current was available prior to the submission.

The pixel matrix consists of a 32×32 pixel array of 50 μm pitch and 6 additional rows of test pixels available at the top of the matrix. Only the 32×32 array was used for these tests: as there are 4 groups of 8 columns, each with a different input transistor and a slightly different collection electrode size [4]. The 16 top rows contain an active reset transistor switched for this purpose, the pixels in the bottom 16 rows contain a diode which absorbs the leakage current from the detector diode and therefore

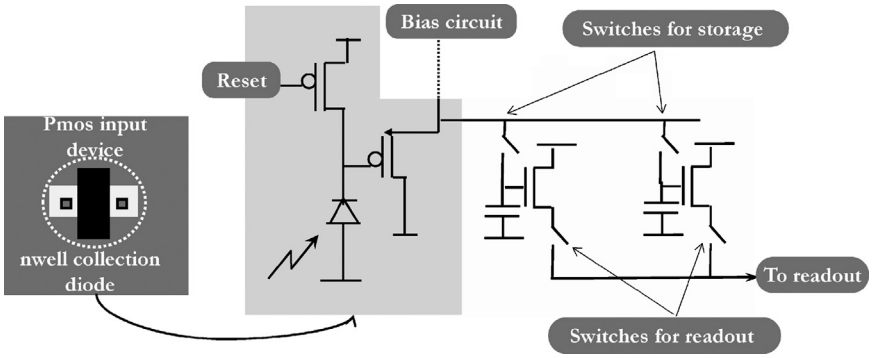

Fig. 2. Pixel circuit.

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