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PARISROC, an autonomous front-end ASIC for triggerless acquisition in next generation neutrino experiments

S. Conforti Di Lorenzo [a,*], J.E. Campagne [a], S. Drouet [b], F. Dulucq [a], M. El Berni [a], B. Genolini [b], C. de La Taille [a], G. Martin-Chassard [a], N. Seguin Moreau [a], E. Wanlin [b], Y. Xiangbo [c]

[a] Laboratoire de l'Accélérateur Linéaire, IN2P3-CNRS, Université Paris-Sud, Bat. 200, 91898 Orsay Cedex
[b] Institut de Physique Nucléaire d'Orsay, IN2P3-CNRS, Université Paris-Sud, 91406 Orsay Cedex, France
[c] Institute of High Energy Physics, Beijing, China.

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ABSTRACT

PARISROC (Photomultiplier ARray Integrated in SiGe ReadOut Chip) is a complete readout chip in AustriaMicroSystems (AMS) SiGe 0.35 μm technology designed to read array of 16 Photomultipliers (PMTs). The ASIC is realized in the context of the PMm2 (square meter PhotoMultiplier) project that has proposed a new system of "smart photo-detectors" composed by sensor and read-out electronics dedicated to next generation neutrino experiments. The future water Cherenkov detectors will take place in megaton size water tanks then with a large surface of photo-detection. We propose to segment the large surface in arrays with a single front-end electronics and only the useful data send in surface to be stocked and analyzed.

This paper describes the second version of the ASIC and illustrates the chip principle of operation and the main characteristics thank to a series of measurements. It is a 16-channel ASIC with channels that work independently, in triggerless mode and all managed by a common digital part. Then main innovation is that all the channels are handled independently by the digital part so that only channels that have triggered are digitized. Then the data are transferred to the internal memory and sent out in a data driven way.

The ASIC allows charge and time measurement. We measured a charge measurement range starting from 160 fC (1 photoelectron-p.e., at PMT gain of 10^6) to 100 pC (around 600 p.e.) at 1% of linearity; time tagging at 1 ns thanks to a 24-bit counter at 10 MHz and a Time to Digital Converter (TDC) on a 100 ns ramp.

1. Introduction

The PMm2 project with the complete title "Innovative electronics for photo-detectors array used in high energy physics and astroparticles" [1] has been conceived in 2005 thanks to the collaboration of three French laboratories (LAL Orsay, LAPP Annecy, IPN Orsay) and the Photonis Company. This project, considering the need of the future underground detectors to reach large dimensions (ten times the Super-Kamiokande detector) [2], proposes to segment the large surface of photo-detection into macro pixels consisting of an array ($2 \times 2\ m^2$) of 16 12 in. PMTs (Fig. 1). Each array is connected directly at its back to an autonomous front-end electronics, which works in a triggerless data acquisition mode. The array is powered by a common high voltage and only one data cable for each one allows the connection by network to the central data event builder and filter.

The PMm2 program has concentrated its research on few subjects [3] such as

- development of the front-end electronics (ASIC and front-end card),
- improvement of the 12 in. PMTs,
- cables,
- data transmission and the DAQ,
- realization of a final $2 \times 2\ m^2$ demonstrator equipped of 16 PMTs.

The micro-electronics group (OMEGA) from the LAL at Orsay was in charge of the front-end electronics and has developed an ASIC called PARISROC (Photomultiplier ARray Integrated in SiGe ReadOut Chip) [4].

The ASIC PARISROC is a complete read-out chip that integrates 16 independent and self triggered channels to achieve charge and

* Corresponding author. Tel.: +33 1 64 46 82 87.
E-mail address: conforti@lal.in2p3.fr (S. Conforti Di Lorenzo).

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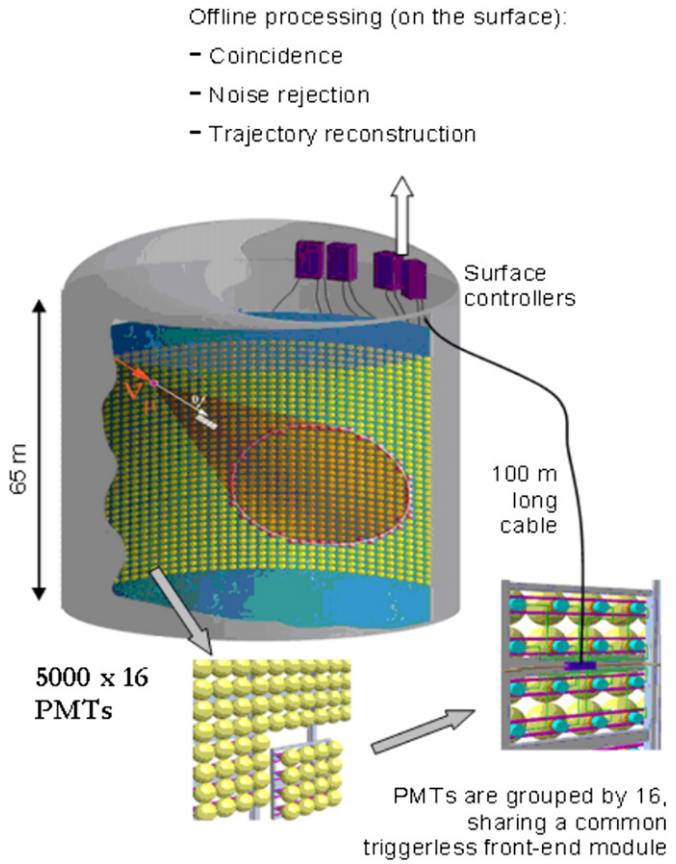

Fig. 1. Principle of PMm2 proposal for megaton scale Cherenkov water tank with a module with 16 PMT.

time measurements. A first prototype [5,6] was produced in 2008 showing the capabilities of a complete self-trigger-digitizer read-out chain. A second chip version has been developed in 2010 to improve the ASIC performances in terms of

- hit rate, by reducing the ADC resolution and by multiplying the read-out frequency by a factor 4 (from 10 MHz to 40 MHZ);
- time measurements thanks to a new TDC structure [6] [7];
- noise and coupling signals by a new input stage structure and a study of the layout floorplan.

This paper describes the second version chip in detail and gives the measurement results.

2. PARISROC architecture

The ASIC PARISROC is a complex SoC (System on Chip) that processes the analog signals up to digitization.

The chip integrates many functions as it needs to auto-trigger asynchronously on any single photoelectron and provides digitized time and charge outputs. It has 16 channels that work independently and are managed by a common digital part. The chip specifications are the following:

- variable gain to use a common high voltage for the 16 PMTs;
- external 50 Ω input impedance to terminate the PMT cable to the ASIC;
- auto-trigger on 50 fC (1/3 of photoelectron at PMT gain of 10^6);
- charge measurement up to 50 pC (300 p.e.);
- time tagging better than 1 ns (TDC);
- internal conversion.

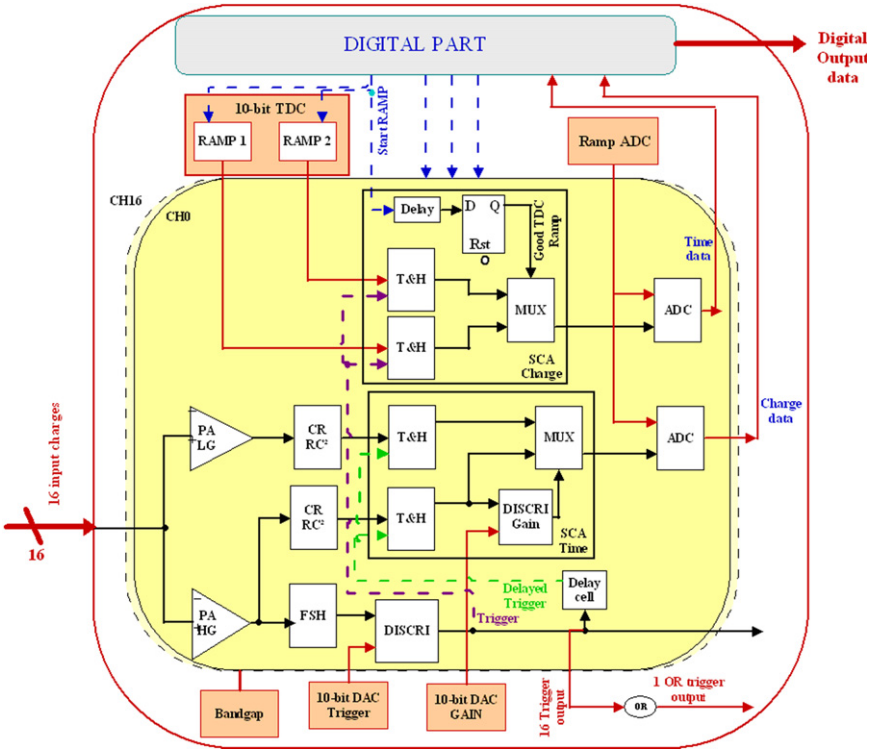

Fig. 2. PARISROC global schematic. The ASIC is represented by a simplified block schematic. Each block is a complex structure. See text for the explanation of the acronyms.