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An acquisition system for CMOS imagers with a genuine 10 Gbit/s bandwidth

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ABSTRACT

This paper presents a high data throughput acquisition system for pixel detector readout such as CMOS imagers. This CMOS acquisition board offers a genuine 10 Gbit/s bandwidth to the workstation and can provide an on-line and continuous high frame rate imaging capability. On-line processing can be implemented either on the Data Acquisition Board or on the multi-cores workstation depending on the complexity of the algorithms. The different parts composing the acquisition board have been designed to be used first with a single-photon detector called LUSIPHER (800 × 800 pixels), developed in our laboratory for scientific applications ranging from nano-photonics to adaptive optics. The architecture of the acquisition board is presented and the performances achieved by the produced boards are described. The future developments (hardware and software) concerning the on-line implementation of algorithms dedicated to single-photon imaging are tackled.

1. Introduction

The CMOS Image Sensors (CIS) are able to provide high-definition images at an ultra-fast frame rate, thanks to the reduction of the grid size (smaller pixels) and the parallelization of the readout lines (column parallel). The further reduction in size trend is not completed and some new techniques for increasing compactness such as 3D integration technology for CIS will provide obviously a huge data flow that is today impossible to treat in-line. The temporary storage solution is more often used when the application allows a sequential readout with an allowed dead time. Nevertheless some real-time applications require an in-line and continuous processing. In this case, the good information has to be extracted from the pixel matrix by applying a data reduction. The CMOS imager such as the electron-bombarded CMOS (ebCMOS) belongs to this category of sensors. Nevertheless, a complicated reduction of data is not easy to implement into a System On Chip (SoC) while keeping versatility. This is true especially for R&D chip for which it is important to keep flexibility through the software of the acquisition system. Indeed, the acquisition system has to be open to different CMOS sensors with analog or digital readout. Furthermore the main board has to sustain a high data throughput and propose an in-line processing. The acquisition system for CIS readout with a genuine 10 Gbit/s bandwidth presented in this paper meets this challenge. This acquisition system is not a pure conceptual attempt on an acquisition system but is driven by low light imaging and single-particle tracking with the ebCMOS camera, LUSIPHER [1].

We present in Section 2, the general architecture of the whole system and the main tasks of each part. Then the heart of the acquisition system, the acquisition boards, is described in Section 3 from an architecture point of view. The implementation and the performances of the boards are discussed in the second part of this section. The software platform developed to overcome some possible limitations of the on board in-line processing is presented in Section 4. To conclude, the future developments (hardware and software) concerning the in-line implementation of the algorithms are tackled.

2. Synoptic of the Data Acquisition System.

The imaging system is composed of 3 main blocks (the ebCMOS camera, the acquisition board and the workstation) and is shown in Fig. 1. In this paper we focus on the acquisition system (DAQ) that is composed of the two last blocks. The ebCMOS detector has been already presented in details in Ref. [1]. The acquisition board is connected to the workstation through a single 10 Gbit/s Ethernet link. It is used both for data acquiring and that for camera control. The DAQ board is connected on the other side to the ebCMOS camera with three different types of communication. The DAQ board receives the analog or digital raw data from the CMOS chip and generates the sequencing patterns to the CMOS chip (clocks, reset). It communicates with the microcontroller inside the camera for the management of the slow control parameters (the configurations

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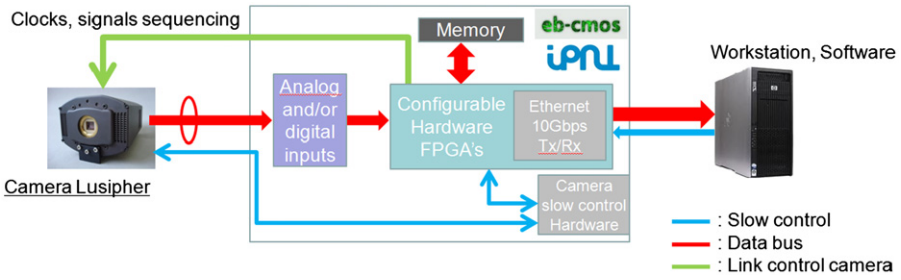

Fig. 1. The ebCMOS imaging system overview with its 3 main blocks: the ebCMOS camera, the acquisition board and the workstation.

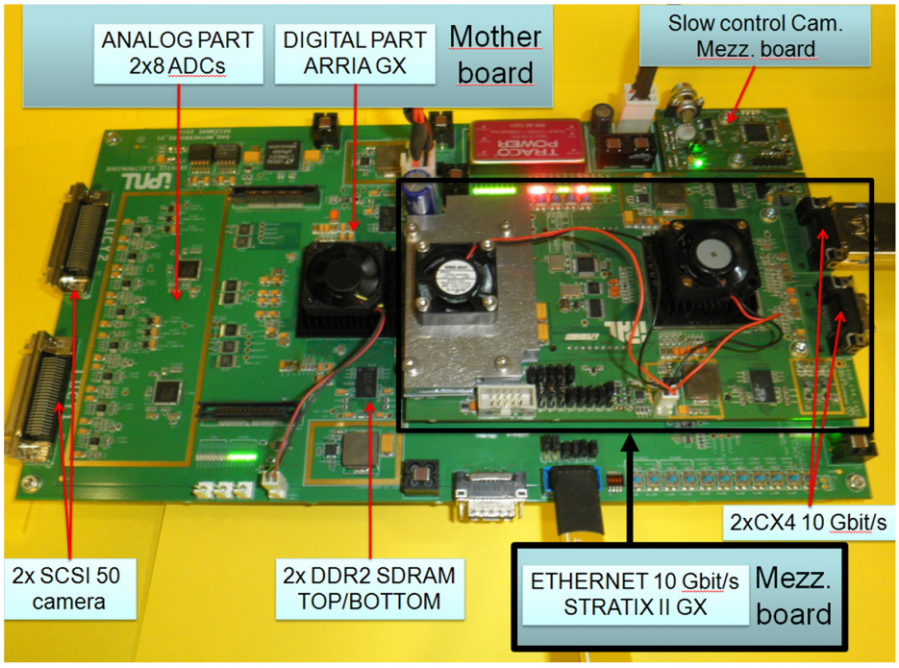

Fig. 2. The DAQ boards: the motherboard with the analog and digital parts, the ComEth10 board with the two parallel CX4 Ethernet links and the smaller board (top right) for the slow control.

of the chip, the reference voltages, the temperatures, the ebCMOS high voltage reference, the hygrometry measurement). In addition to I/O management, the DAQ board digitizes the 16 analog signals in parallel (65 MHz/channel) and performs some simple imaging processing (the Correlated Double Sampling computation and the pedestal subtraction). The software, the third block, runs on a multi-core workstation equipped with a 10 Gbit/s Ethernet board and a Solid State Disk for data storage on the fly.

The software also has an interface to the end-user through a Graphical User Interface implemented in Qt language. The DAQ software implements algorithms for in-line pattern recognition dedicated to single particle tracking based on single-photon detection. The noise suppression algorithms are also implemented to increase the image quality. The DAQ system works continuously with the ebCMOS camera LUSIPHER (800×800 pixels), at a frame rate of 500 Hz and all implemented algorithms in parallel.

3. DAQ boards

The DAQ board has been designed to be modular and is opened to other CMOS chips than the LUSIPHER ebCMOS. It is composed of three electronic boards. The motherboard is dedicated to the digitization, to pattern generation and for raw data processing (CDS). One of the 2 daughter boards (ComEth10G) is the communication card to the workstation through two parallel 10 Gbit/s Ethernet links (2×10 Gbit/s bandwidth upgrade is possible). This board can be used in addition for data processing, thanks to memory banks connected to a powerful FPGA. The second daughter board is devoted to the slow control of the camera. The picture of the 3 boards assembly is shown in Fig. 2.

3.1. Architectures

3.1.1. Motherboard

The motherboard is connected to the LUSIPHER camera with two SCSI (50 pins). Those links allow on one hand to the transmission of the patterns generated by the FPGA such as the clocks and the resets required for the sequencing of the CMOS chip and on the other hand to the reception of the analog signals coming from the pixel outputs. The board has 16 analog inputs for a parallel digitization by the 12 bit ADCs [2]. The sampling clock can be tuned on the pixel clock for an optimized sampling (40 MHz for the ebCMOS LUSIPHER) with a maximum sampling frequency of 65 MHz. In this last case the sampling rate is 1.04 GS/s. This corresponds to a maximum input data flow for the FPGA of 12.48 Gbit/s. In case of the LUSIPHER ebCMOS, the input data rate obtained for 800×800 pixels, 16 outputs in parallel and a 40 MHz clock is 7.68 Gbit/s. The motherboard can