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Implementation of a neural network for digital pulse shape analysis on a FPGA for on-line identification of heavy ions

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A B S T R A C T

Pulse shape analysis techniques for the identification of heavy ions produced in nuclear reactions have been recently proposed as an alternative to energy loss and time of flight methods. However this technique requires a large amount of memory for storing the shapes of charge and current signals. We have implemented a hardware solution for fast on-line processing of the signals producing the relevant information needed for particle identification. Since the pulse shape analysis can be formulated in terms of a pattern recognition problem, a neural network has been implemented in a FPGA device. The design concept has been tested using ^{12,13}C ions produced in heavy ion reactions. The actual latency of the system is about 20 μs when using a clock frequency of 50 MHz.

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1. Introduction

Radioactive beam facilities provide a unique tool to investigate nuclear structure and dynamics by exploring the isospin degree of freedom. There are several new facilities foreseen to be operative in the near future, like SPIRAL2 at GANIL (France), FAIR at GSI (Germany) or SPES at LNL (Italy). They will accelerate radioactive nuclear beams with large intensities allowing for the study of short-lived nuclei not presently available. These studies demand very powerful detection systems, including full identification of reaction products over the largest dynamical range and with the lowest possible thresholds.

The principle of operation of commonly used radiation detectors is based on the conversion of the energy deposited by the particles impinging in the detector into an electric signal. The time dependence of the current (or charge) signals depends on the (Z, N) values of the reaction fragments, mainly due to the differences in the carrier density created along their path through the detector bulk. This feature becomes the basis of pulse shape analysis techniques (PSA) developed for particle identification systems [1–5]. The process of identification of the shape of the signal produced by charged particles in the detectors is actually a pattern recognition problem. The basis of pattern recognition has been extensively studied in the last twenty years. One of the most popular classes of algorithms is the so-called "artificial neural network" (ANN) [6,7].

When the experimental scenario makes PSA identification mandatory, an off-line analysis procedure can be implemented after storing the shapes in a convenient digital media. Typical pulses can be as large as 200 ns for heavy fragments, and good results have been obtained with a 125 MHz sampling rate [8]. However, when experimental rates approach the kHz level per detector, fast data transfer and large storage memory devices are required. On the other hand, digital signal processing algorithms have become more powerful while advances in modern integrated-circuit technology provide compact, efficient ways of implementation. The degree of development achieved presently by modern digital technologies makes them quite attractive for applications in nuclear physics detectors, where good timing and energy performances are simultaneously demanded. In particular, an on-line hardware solution providing fast PSA analysis will drastically reduce the size and complexity of the system.

The use of modern FPGAs and microprocessors allows the development of a data processing system that can be easily adapted to the particular needs of the experiment. In addition, the FPGA architecture is particularly suitable for the ANN implementation that is described in this work. For the purpose of the present work, we have chosen a simple FPGA device model Spartan 3AN700 [9], taking advantage of its low cost and high configurability; our main purpose is to test the viability of the

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design concept. The FPGA option in fact provides the flexibility needed to test and optimize different ANN architectures and characteristics. Another important advantage of FPGA devices is their relative radiation hardness as compared to microprocessors or other programmable devices, so they could be more suitable for designing a dedicated Front End Electronics (FEE) for particle detectors systems needed in nuclear physics spectroscopy.

Here we report on a prototype of front-end electronics capable of performing PSA analysis of energetic heavy ions ($\sim$10 MeV/u) impinging on surface-barrier silicon detectors. The paper is organized as follows: In Section 2 we present general system requirements and the methodology used in our studies. In Section 3 we treat the main blocks of the ANNs employed for particle identification. In Section 4 we discuss the specific details of FPGA programming and the application to ^{12,13}C identification. Finally, the conclusions of our work are summarized in Section 5.

2. Requirements and methodology

The typical architecture of a data acquisition system for a particle detector is shown in Fig. 1. The detector, which may be well a pixel or strip detector, acts as a capacitor collecting the charge produced by the impinging particles until they stop in the bulk of the material. The PSA technique uses the time distribution ("shape" from now on) of the charge collection (current signal) to extract the relevant parameters needed to identify the impinging ion. Although different radiation sensitive materials will produce different amplitudes, in general terms charge deposition per unit time is small and should be amplified in order to record the shape of the physical event. This process is carried out by the combination of a wide-band preamplifier ($\sim$300 MHz) and a digital system. Finally, a digital pre-processing is performed to classify and analyze the pattern before transferring the identification information to the data storage unit. This is the so-called "pulse shape analysis" technique.

While in the commonly used off-line analysis each complete event must be processed, our approach is intrinsically parallel and the segmentation of the detector can be efficiently exploited for a parallel partial analysis of the entire event. In this scenario, a multiplexing scheme must be implemented in the FPGA to handle the data flow toward the output device (storage or subsequent stages of the data acquisition chain) as schematically shown in Fig. 1. Therefore, when dealing with a particle impact-rate around a few kHz, the bottleneck will be in the communication with the output device and not in the on-line analysis process. Multiple hit events are not considered at present configuration but can be easily implemented.

In our design, the digitized signal shapes coming from the detector are fed serially to the ANN, along with a protocol signal indicating that the sample is valid.

One of the main features of neural networks is their learning ability. In particular, in this work we use a Multilayer Perceptron neural network (MLP). The training stage is performed off-line, where a set of real numbers (weights) are provided to each neuron. This process must be carried out using realistic signal shapes of heavy ions. We have implemented a network with two neuron output layer, which seems to be sufficient to classify a wide range of heavy ion shapes, as it is discussed in Section 4. However, the designed MLP is fully reconfigurable in its architecture (number of neurons and their distribution in layers), the number and size of input data, so that it can be adapted to the different experimental conditions.

The high flexibility of the FPGA architecture in fact allows us to describe a generic fully configurable MLP using a VHDL code (VHSIC Hardware Description Language). The configuration data are the architecture of the MLP and its data size (numerical format). In the process of network training, which can be accomplished using typical heavy ion pulse shapes in the reactions under study, the performances of different architectures involving various combinations of layers and neurons are tested to determine the optimal configuration and the corresponding weights. This task is performed off-line with a software tool, such as Matlab.

The numerical format will be determined by weight values and by the resolution of ADC, considering a fixed-point arithmetic. The size of the integer part is determined by the weights, whereas the size of the decimal part is determined by the resolution of the ADC. If the experimental conditions impose a change of the configuration data, a new implementation of the system (hardware) has to be built. However, a change of the weights would only require a reprogramming of the device.

3. Implementation of the neural network

One of the advantages of a neural network is its high degree of parallelism, but this mode of operation requires large hardware resources and FPGA devices are usually very limited. Therefore, most of the implementations of MLP's in FPGA's are performed serially. In this case a single neuron must perform as many iterations as the number of neurons composing the full MLP. For an optimal use of the FPGA hardware implementation resources, however, one can implement in a single device several MLP's with a larger number of dedicated neurons. In this case, the number of iterations is given by the ratio between the neurons in the MLP and total number of neurons implemented. The basic structure of this implementation is shown in Fig. 2.

The input shift register stores the input data. These and the weights (previously stored in a memory) are fed to the neurons to perform the MLP operation. The output of ANN neurons is handled by a dedicated output shift register. The group of operations performed by each component is driven by the controller.

3.1. Input shift register

The input stage consists of two shift register. The first register stores the input data, and the second register loads the temporary data produced by the neurons at each layer. The output port must be connected to each register depending on the layer currently in

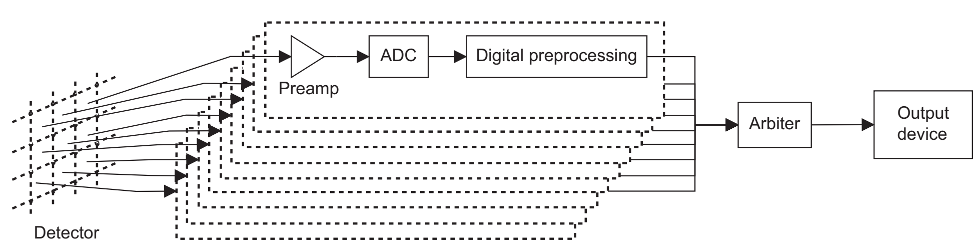

Fig. 1. Block diagram of a typical electronic chain for PSA. The signal from detector is amplified for a charge sensitive amplifier, then is converted into bits by an ADC, and finally digitally processed.

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