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Effect of substrate and temperature on the electronic properties of monolayer molybdenum disulfide field-effect transistors

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ABSTRACT

The use of two-dimensional nanostructured molybdenum disulfide (MoS_2) films in field-effect transistors (FETs) in place of graphene was investigated. Monolayer MoS_2 films were fabricated by chemical vapor deposition. The output and transfer curves of supported and suspended MoS_2 FETs were measured. The mobility of the suspended device reached 364.2 $cm^2\,V^{-1}\,s^{-1}$ at 150 °C. The hysteresis of the supported device in transfer curves was much larger than that of the suspended device, and it increased at higher temperatures. These results indicate that the device mobility was limited by Coulomb scattering at ambient temperature, and surface/interface phonon scattering at 150 °C, and the injection of electrons, via quantum tunneling through the Schottky barrier at the contact, was enhanced at higher temperatures and led to the increase of the hysteresis. The suspended MoS_2 films show potential for application as a channel material in electronic devices, and further understanding the causes of hysteresis in a material is important for its use in technologies, such as memory devices and sensing cells.

1. Introduction

Two-dimensional layered crystalline materials with atomic-scale thickness have received intense interest in recent years. Graphene is a well-known example of such a material, and has been used in radio-frequency analog transistors with cut-off frequencies that reach hundreds of gigahertz because of its high carrier mobility [1–3]. However, pristine graphene is a zero-bandgap semiconductor with a high off-state current, which limits its use as a material for digital logic transistors [4]. Bulk molybdenum disulfide (MoS_2) is a semiconductor with an indirect bandgap of 1.2 eV, while a monolayer of MoS_2 has a direct bandgap of 1.8 eV. Therefore, MoS_2 is a promising alternative to graphene for use in logic circuits [5,6]. Modulation of the band structure, and electronic and magnetic properties of isolated MoS_2 monolayers and bilayers has been the subject of numerous theoretical and experimental investigations [7]. Additionally, the n-type mobility of mechanically exfoliated monolayers of MoS_2 on SiO_2 at ambient temperature is < 10 $cm^2\,V^{-1}\,s^{-1}$. This is substantially lower than the calculated value for intrinsic n-type MoS_2 monolayers (410 $cm^2\,V^{-1}\,s^{-1}$), which is limited by optical phonon scattering [8,9]. However, mechanical exfoliation cannot be scaled up for commercial applications [10]. Chemical vapor deposition (CVD) is a more scalable process for producing thin films than mechanical exfoliation.

The unique band gap characteristics of this material makes it suitable for low power and high on/off ratio electric and photoelectric devices [11–13]. However, its inherent hysteresis introduces instability in devices. To understand the origin of the hysteresis in MoS_2, its surface has been assumed to be the origin of the hysteresis. A number of parameters, including gate voltage, sweep time, range and direction were varied while the hysteresis was monitored [14]. Extrinsic hysteresis effects are often observed in MoS_2 field devices, for instance, charge trapping is assumed to be one cause of hysteresis in MoS_2 based devices [15,16]. Additionally, it has been shown that the adsorption of moisture or gases on the surface of MoS_2 can lead to hysteresis [17,18], while others have shown that charge traps at the interface of MoS_2 and the SiO_2 substrate cause the hysteresis [19]. Late et al. reported the origin of MoS_2 field effect transistors hysteretic and transient behaviors and suggested that hysteresis was largely due to absorption of moisture on the surface and intensified by high photosensitivity of MoS_2 [20]. The findings of Shu et al. indicated that the hysteresis comes from the MoS_2 itself, revealing an intrinsic origin of the hys-

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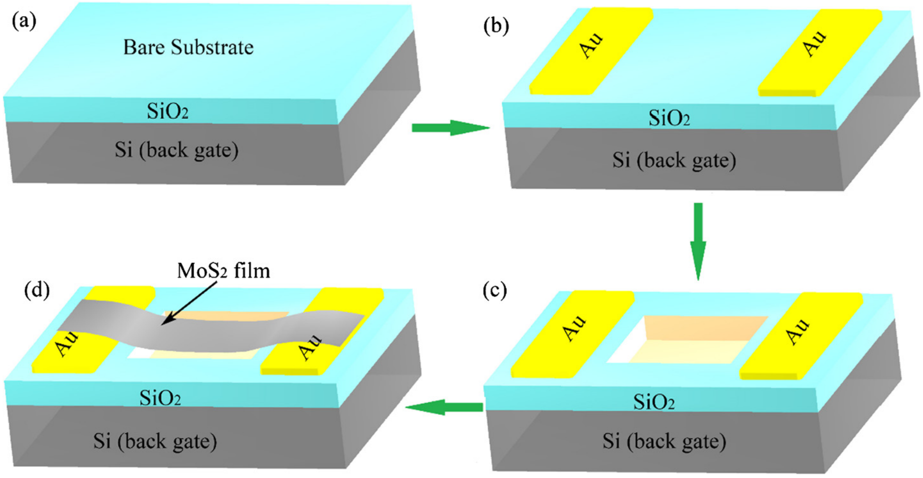

Fig. 1. The suspended FET fabrication process. (a) The bare Si substrate with 300 nm SiO_2, (b) Ti/W and Au were deposited onto the SiO_2 for the source and drain electrodes, (c) holes were fabrication on the substrate for the suspended devices, (d) MoS_2 film were transferred on the substrate.

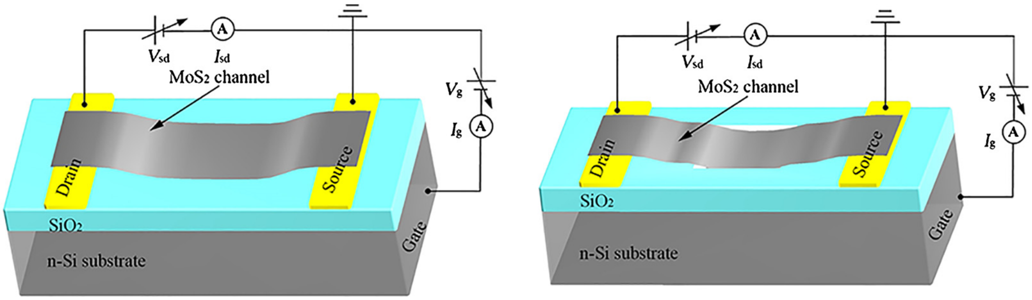

Fig. 2. Schematic diagram showing the device architecture of the supported (a) and suspended (b) MoS_2 FETs.

teresis besides some extrinsic factors [21]. Shimazu et al. reported the effects of environmental gases on the transport properties of back-gated multilayered MoS_2 field-effect transistors. Comparisons between different gases (oxygen, nitrogen, and air and nitrogen with varying relative humidities) revealed that water molecules acting as charge-trapping centers were the main cause of hysteresis in the transfer characteristics [22]. Although there are many reports on the hysteresis in MoS_2 field effect transistors (FETs), the reasons for the observed hysteresis is not well understood.

The majority of MoS_2 FETs are fabricated by mechanical exfoliation. Techniques that allow the fabrication of large area MoS_2 films, including CVD, have developed rapidly. This has made the use of MoS_2 in practical electronic devices possible. Importantly, if the hysteresis behavior of this material was understood and controlled, MoS_2 can be incorporated into high performance devices, including integrated flexible circuits or chemical sensors [23,24]. Our study is an important advance in the development of MoS_2 FETs, an essential step towards achieving high-performance and low-power nanoscale electronics and optoelectronic devices.

2. Experimental detail

Devices were fabricated with a MoS_2 layer either supported or suspended over a Si/SiO_2 substrate composed of SiO_2 (300 nm) with a highly n-doped Si substrate as the back gate. The fabrication of the devices is outlined in Fig. 1. Silicon (Si) substrates were coated with thermally grown silicon dioxide (SiO_2, 300 nm) as shown in Fig. 1(a). The substrates without square holes were prepared for the supported devices and the substrates with square holes for the suspended devices. TiW (5 nm) and Au (100 nm) were then deposited under vacuum through stencil masks onto the SiO_2 for the source and drain electrodes, respectively (Fig. 1(b)). The square holes were created in the substrate for the suspended device (Fig. 1(c)), with the holes of 6 μm width and 290 nm depth. The supported FET was fabricated with the substrate without holes.

The process of CVD-grown MoS_2 film was presented as follows. First, the substrate was prepared and the surface was cleaned with ethyl alcohol and deionized water. 0.6 g S powder and 30 mg MoO_3 powder were then weighted and put into the position in tube furnace, respectively. After the tube was full of N_2, the temperature was raised up to 550 °C with the rate of 20 °C/min. Subsequently, the temperature was raised up to 850 °C with a slowly rate 5 °C/min. This temperature was kept with 15 min, and the temperature was cooled to room temperature. Finally the MoS_2 film was generated on the substrate. MoS_2 monolayers were synthesized directly on the Si substrate using CVD and contained single crystals of up to 20 μm in size according to the scale bar in Fig. 3. Polymethyl methacrylate (PMMA) was used to position the MoS_2 films with respect to the substrate to form the MoS_2 FETs. Subsequently, polymethyl methacrylate (PMMA) was used to transfer the MoS_2 films to the substrates, as shown in Fig. 1(d). The PMMA was solved in acetone and then the devices were cleaned in alcohol and deionized water.

A schematic diagram of the supported and suspended FETs are shown in Fig. 2(a) and (b), and the optical images of MoS_2 films are presented in Fig. 3(a) and (b), respectively. As shown in Fig. 3, the geometric configuration of MoS_2 film was triangular, and the size was 20 μm.

Raman spectroscopy was used as a non-destructive method to characterize the crystalline quality and thickness of the MoS_2 sheets [25]. Raman spectra were recorded using a LabRAM HR800 (HORIBA Scientific, Japan) Raman system following excitation at 532 nm. The laser power was kept below 0.25 mW to avoid laser-

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