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Effect of Ni to the Cu substrate on the interfacial reaction with Sn-Cu solder

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ABSTRACT

Both the formation of voids and the growth of a Cu_3Sn layer were suppressed during reactive diffusion between Sn-0.7%Cu solder and Ni added Cu substrates compared with between the solder and a Cu substrate without Ni. The effects of Ni on the formation of voids and of Cu_3Sn were studied using microstructural, thermodynamic and kinetic approaches. Thermodynamic calculations were performed on the assumption where the addition of Ni affected the chemical potential and diffusion driving force at both the Cu-Ni/Cu_3Sn and Cu_3Sn/Cu_6Sn_5 interfaces. The results suggest that the elements (Cu and Sn) in the Cu_3Sn layer are diffuse in opposite directions than normal after prolonged annealing. The results of calculations performed to assess the effects of Ni on elemental diffusion in the Cu_3Sn layer were in agreement with experimental observations. In addition, calculations were performed for scenarios both with and without the presence of $(Ni,Cu)_3Sn$ to understand the role that the addition of Ni plays in decreasing the thickness of the Cu_3Sn layer.

1. Introduction

Power devices are typically made by solder mounting silicon chips on lead frames. Cu-based alloys are used for the frames to ensure reliable connections, because such alloys offer good connection strength as well as suitable electric and thermal conductivity in typical usage environments. Sn-0.7mass%Cu (hereafter referred to as Sn-0.7Cu) solder is a promising candidate to replace the Sn-37mass%Pb typically used for such applications, since it exhibits a high melting point (~500 K) and good solderability in commercial processes. It is well known that the interfacial reaction layers formed between the Cu-based lead frame and the Sn-0.7Cu solder are composed of Cu_3Sn and Cu_6Sn_5, both of which are equilibrium phases. During prolonged annealing, voids are formed at the Cu/Cu_3Sn interface, resulting in decreased reliability of the device. This effect is often attributed to the formation of Kirkendall voids resulting from the different diffusion rates of Sn and Cu at the interface [1–2]. In order to avoid these defects, Ni-plated Cu lead frames are sometimes used for the fabrication of electronics, due to the presence of a Ni diffusion barrier at the interface. However, since the associated plating process drives up the cost of production, plating-free processes are still desirable.

If these defects are indeed Kirkendall voids, it may be possible to avoid their appearance by alloying elements with the solder or Cu lead frame, since it has been demonstrated that alloying elements with the solder significantly affects the growth of intermetallic compounds (IMCs) [3–7]. As an example, Nishikawa et al. have reported the effect of adding Ni to Sn–Cu solder on the interfacial reaction between the solder and a Cu substrate [3]. They observed that the growth of IMCs after aging was suppressed when adding a small amount of Ni (0.05 mass%) to the solder. However, it has also been confirmed that alloying other elements with the Cu lead frame can greatly modify IMC growth [8–10]. Takemoto et al. have reported the effect of additional elements in the Cu substrate on the growth of IMCs by the interfacial reaction between a Sn–Pb solder and a Cu-X alloy [8]. This work found that the addition of 1 at.% X (X = Mn, Ni or Ag) to the Cu substrate decreased the total thickness of the IMCs following annealing at 423 K. In contrast, voids and cracks were observed when Ni-containing Cu alloys were soldered with Sn–Pb. Vuorinen et al. demonstrated interfacial reactions between Sn and Cu-x%Ni alloys (at.%, x = 0, 0.1, 1.0, 2.5, 5.0, 10) annealed at 398 K [9]. The thickness of the Cu_3Sn decreased as a function of increasing Ni content and no Cu_3Sn was observed upon the addition of 10% Ni to the Cu. The addition of 1 to 2.5% Ni generated a number of voids at the Cu/Cu_3Sn interface, while these voids were not observed when adding 5 to 10% Ni. Vuorinen et al. discussed these phenomena based on thermodynamic and microstructural effects [9]. In general, it has been shown that the driving forces responsible for the diffusion and mobility of the various elements are altered by the dissolution of Ni in the IMCs, resulting in varying IMC growth behavior as well as changes in void formation.

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As described above, the addition of Ni to the solder or the Cu substrate has significant effects on the thickness of the IMCs and the formation of voids. In previous studies, however, there is currently an insufficient understand of the growth behavior of IMCs as well as the void formation mechanism. A further analysis of the Cu substrate/Cu_3Sn interface will be needed because that interface is believed to be the region at which voids emerge during annealing [4–11]. In the present study, we investigated the relationship between the Ni content in the Cu substrate and the percentage of voids and the IMC thickness. We also examined the interfacial reaction at the Cu-Ni/Cu_3Sn interface in detail using transmission electron microscopy (TEM) and considered the thermodynamics of the Sn-Cu-Ni alloy system in order to clarify the effect of adding Ni to the Cu substrate on the growth of Cu_3Sn and on the diffusion of Cu and Sn.

2. Experimental procedure

Cu-x%Ni-2%Sn-0.15%Zn-0.006%P alloys (mass%, x = 0.09, 0.2, 0.4) were used as the Cu substrates (hereinafter referred to as the Cu alloy) of 2 mm × 25.4 mm × 25.4 mm (MITSUBISHI ELECTRIC METECS). Sn and Zn was added to enhance strength and P was added for deoxidation. Mirror surfaces were prepared on Cu alloy specimens by mechanical polishing and electropolishing with 20% sulfuric acid, following which a 0.08 mm thick Sn-0.7Cu solder foil (SENJYU METAL) were set on top of the Cu alloy. The soldering was carried out at 553 K for 300 s under nitrogen containing 4% hydrogen. After soldering, the samples were annealed at 423 K for 1000 and 2000 h (3600 and 7200 ks), respectively. The aging condition at 423 K for 1000 h is commonly used as an accelerated storage test for microelectronic assemblies [2]. The microstructures of samples were observed by scanning electron microscopy (SEM Hitachi High-Tech S-4800).

The configuration of the interface at which the voids emerge varies over time. In addition, the connection status of the interface between Cu alloy and Cu_3Sn layers is an important factor affecting the prescribed properties such as strength, electric and thermal conductivity. Therefore, the void proportion was defined as the ratio of the void length to the total observed length projected to the Cu alloy/Cu_3Sn line, as illustrated in Fig. 1. The total observation length was 25 μm and three SEM micrographs in each sample of three samples were used to determine each void proportion. The Cu_3Sn and Cu_6Sn_5 thicknesses were measured over 2 μm intervals using the same SEM images. In order to accelerate the interfacial reaction to allow detailed observations of the Cu/Cu_3Sn interface at which the voids emerge, the soldered samples were annealed at 473 K for 700 h (2520 ks). Foils for TEM (JEOL JEM-2100F) were prepared by focused ion beam machining. Detailed microstructure observations at the Cu–Ni alloy/Cu_3Sn interface were performed using TEM equipped with an energy disperse spectroscopy (EDS) detector (EX-24063JGT).

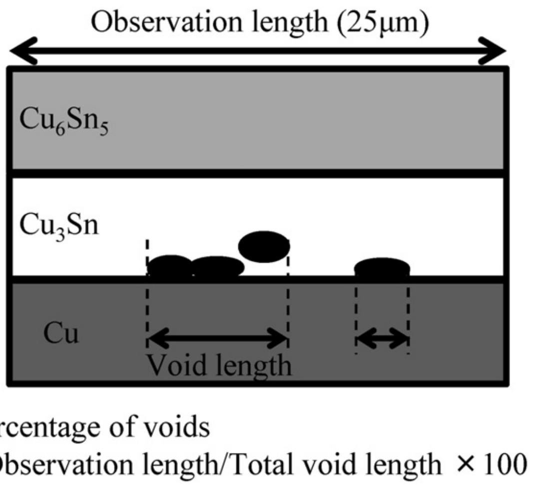

Fig. 1. Schematic illustration of calculating void percentages.

A metastable phase diagram assuming local equilibrium of chemical potential was constructed via calculations using the Thermo-calc software package (Ver. S) together with thermodynamic data for the Cu-Sn-Ni system obtained from previous work and from the literature [13–20]. The influence of Zn and P were excluded from the thermodynamic and kinetic approaches because of thermodynamic data for the Cu-Sn-Ni ternary system. The chemical potential can be calculated with ease when local equilibrium is assumed at interfaces. Simply as an example, when Gibbs energy curves of FCC and Cu_3Sn at 423 K are calculated, a common tangent line of these curves can be drawn. The intersections of y-axis at 0% and 100% are the chemical potentials of Sn and Cu at the FCC/Cu_3Sn interface, respectively. Details of the calculation for the chemical potential were reported in the previous study [11] and other work [12,16]. A discussion of the calculation model and methods are provided in Sections 4.1 and 4.2.

3. Results

3.1. Effect of adding Ni to the Cu alloy on the formation of voids and IMCs

Fig. 2 shows SEM images of samples annealed at 423 K for 2000 h. Both Cu_3Sn and Cu_6Sn_5 are clearly present in these specimens, regardless of the Ni content in the Cu alloy. When Ni-free Cu alloy was used for the substrate, as in Fig. 2a, a large quantity of voids was uniformly distributed over the sample, connected together and primarily located at the Cu/Cu_3Sn interface. Based on these figures (a)–(d), the amount of voids evidently decreased with increasing Ni content in the Cu alloy. The relationship between the Ni content and the percentage of voids is shown in Fig. 3a, from which it can be seen that the void content decreased with increasing Ni content and that there is a significant variation in the void content up to 0.2% Ni. In ref [2], voids were substantially not observed when high purity oxygen free copper (OFHC-Cu) was used as a substrate. However, the voids were observed when Ni-free Cu alloy was used as a substrate in this study, which suggests that the alloying element such as Sn, Zn and P in the substrate might accelerate the formation of the voids. Alternatively, since the substrate was electro-polished, we cannot deny the effect. In any cases, the formation of voids was suppressed by using Ni added Cu substrate, although a large quantity of voids was formed when the substrate without Ni was applied. It is obvious that addition of Ni significantly affects the diffusion fluxes behavior which was the cause of the voids formation. Accordingly, the problem could be solved by using microstructure analysis and thermodynamic approaches. Fig. 3b summarizes the effect of Ni content on the Cu_3Sn and Cu_6Sn_5 thicknesses and on the total IMC thickness ($Cu_3Sn + Cu_6Sn_5$). The Cu_3Sn thickness decreased with increasing Ni content. Conversely, the thickness of the Cu_6Sn_5 layer increased with increasing Ni content, demonstrating that even a small amount of added Ni (0.09%) was effective at promoting the growth of Cu_6Sn_5. The addition of Ni contributes to a decrease in the Cu_3Sn thickness and also increases the Cu_6Sn_5 thickness. Since the total thickness change results from a combination of these two effects, the maximum thickness is obtained on adding 0.09% Ni, after which a slight decrease is observed on further addition. As stated in the Introduction, one cause of void formation is the Kirkendall effect, and so a certain degree of correlation was observed between void formation and the IMCs, regardless of annealing time and Ni content. Fig. 4 plots the relationship between the percentage of voids and the Cu_3Sn and Cu_6Sn_5 thicknesses of samples annealed at 423 K for 1000 h or 2000 h. Here a strong positive correlation is demonstrated by the R^2 value of 0.85 for the plot between the percentage of voids and the Cu_3Sn thickness, as shown in Fig. 4a. In contrast, a moderately strong negative correlation ($R^2 = 0.56$) was observed between the percentage of voids and the Cu_6Sn_5 thickness (Fig. 4b). In addition, there was very little correlation ($R^2 = 0.05$) between the percentage of voids and the total thickness. These results