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A CMOS transimpedance amplifier with high gain and wide dynamic range for optical fiber sensing system

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ABSTRACT

For the optical fiber sensing applications, a new CMOS transimpedance amplifier (TIA) with high gain and wide dynamic range has been designed based 0.18 μm CMOS process. The TIA proposed consists of three-stage cascade push pull inverter, inductive-series peaking, automatic gain control (AGC) circuit, signal to differential circuit, and output buffer. Three-stage cascade push pull inverter is used to achieve enough high gain. The inductive-series peaking technique is employed in this design to extend further the bandwidth. Automatic gain control circuit is used to realize wide dynamic range. In order to reduce the signal reflection, output buffer is added in this design. Owing to the signal output of three-stage cascade push pull inverter and the differential inputs of output buffer, Single to differential circuit must be set in the design to complete the matching.

1. Introduction

Recently, a method of using an optical fiber as a sensor for detecting, for example, ground deformation, the distortion or deformation of a structure, etc., has been proposed. Fig. 1 shows the optical fiber sensing system which mainly includes optical source, transmission optical fiber, sensing head, photodetector, and signal processing module. In this system, a transimpedance amplifier (TIA) is used widely as the front-end of signal processing module to convert the small photocurrent from the photo-detector to an amplified voltage signal. Therefore, the TIA has better possess a high gain. At the same time, it should have a wide dynamic range (DR) and low noise because the large input photocurrent saturates the TIA and makes it insensitive to the input signal [1].

To process the weak photocurrent signal, TIA gain is needed to be large enough. In practical optical fiber sensing applications, the TIA does not always operate a nearby sensitive case, i.e., handling the lowest input signal considered. When high input signals are processed, saturation might occur and degrade the output signal significantly. DR is here defined as the ratio of maximum-to-minimum input photocurrent which can still be sensed by TIA. And DR is mainly determined by the feedback loop of the TIA. However, the feedback loop also affects the transimpedance gain and the bandwidth of TIA. The improvements of these demands may be contradictory. Therefore, a trade-off should be taken into account among them. In order to protect the TIA from saturation and improve the input current overdrive capability, the full input photocurrent range is divided into two regions to improve the dynamic range [2]. Moreover, the 2-stage compression concept has been described [3]. On the basis of the concept, the full input current range is separated into three regions in this design: inactive, one-active and both-active thus further broadening the DR and increasing the input current overdrive capability.

The sensitivity is defined that the acceptable mean minimum optical power at the specified bit error ratio (BER). And the sensitivity S can be expressed as:

$$S = \frac{Q\sqrt{I_{\text{nin}}}}{R_0} \tag{1}$$

where the Q is the noise distance determined by the signal current and input noise current. For a typical value BER of 10^{-9} in practice, the value of Q is equal to 6. I_{nin} is the total input noise current, and R_0 is the responsivity of the photodetector. For a high speed photodetector, the responsivity is very small (typically 0.04 A/W), which requires more stringent noise performance to obtain high sensitivity [4].

Currently, the work on the TIA presents two trends: one is resolving the bottleneck of the bandwidth, and the other is optimizing the sensitivity and dynamic range [5]. In this design, an

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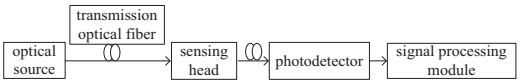

Fig. 1. The block diagram of optical fiber sensing system.

AGC circuit is used to achieve a wide DR. Besides, a shunt transistor is also employed to further enlarge the DR. Based on the previous work [6], the AGC circuit is improved by using peak detector, level shifter, and buffer instead of the MOS transistor and resistor in series. The parallel feedback resistor is replaced by a MOS transistor. So the process variation can be reduced effectively and the dynamic range becomes wider. In order to reduce the signal reflection, output buffer is added in this design. Single to differential circuit is employed to realize the matching of signal output to differential inputs.

2. Circuit implement

The diagram of the whole transimpedance amplifier circuit is shown in Fig. 2. The TIA proposed consists of three-stage cascade push-pull inverter, automatic gain control (AGC), inductive-series peaking, single to differential circuit, and output buffer. The three-stage cascade push-pull inverter is the core of the TIA, and AGC can adjust the gain of the core according to the input signal amplitude. The subsequent block of output will provide a fully differential 50 Ω output driver and reduce the signal reflection.

Three-stage cascade push pull inverter is used to achieve the gain in demand. In order to extend further the bandwidth, the inductive-series peaking technique is used in this design. Fig. 3 shows the circuit structure of three-stage cascade push-pull inverter with inductive-series peaking. Three-stage cascade push-pull inverter is comprised of M_1–M_9 transistor. The PMOS and NMOS transistors in the push pull inverter can be both biased in saturation region to maximize the transconductance and increase the gain bandwidth product of the entire structure [7]. The voltage drop of the feedback resistor R_f can provide the bias voltage for MOS transistors without an additional bias source and regulate the input matching. The transistor M_3, M_6, and M_9 serve as active load so that the amplifier transistors can enlarge their sizes to avoid overshoot. Moreover, it can also increase the bandwidth and minimize the Miller effect. The inductive-series peaking technique is

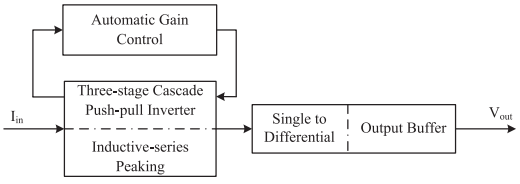

Fig. 2. The overall circuit diagram.

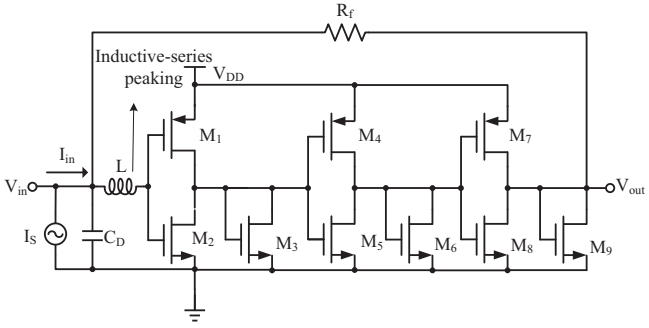

Fig. 3. Three-stage cascade push-pull inverter with inductive-series peaking.

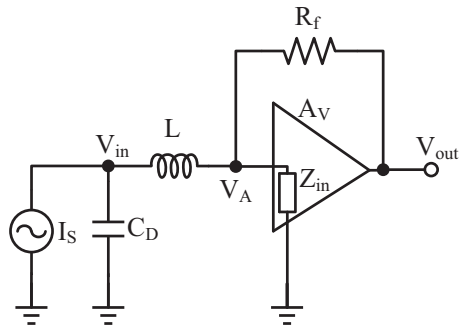

Fig. 4. The simple equivalent model of three-stage cascade push-pull inverter with inductive-series peaking.

realized by the inductor L inserted into the input terminal of three-stage cascade push pull inverter. Compared with the active inductor [8] which normally consists of a MOS transistor and a resistor, the off-chip spiral inductor L used in this design can provide a higher inductance value in the low-voltage high-speed circuits.

The dominant pole of three-stage cascade push pull inverter lies in the input terminal. The transimpedance gain AR can be expressed as [9]

$$A_R = \frac{V_{\text{out}}}{I_{\text{in}}} \approx R_f \tag{2}$$

The −3 dB bandwidth without inductive-series peaking can be expressed as [10]

$$f_{-3\,\text{dB}} = \frac{A_{\text{total}}}{2\pi R_f C_{\text{in}}} \tag{3}$$

where C_{in} is the input capacitance of three-stage cascade push pull inverter. A_{total} is the total voltage gain.

$$A_{\text{total}} = A_{V1} \times A_{V2} \times A_{V3} \tag{4}$$

where A_{V1}, A_{V2}, A_{V3} are respectively the voltage gain of the first stage, the second stage and the third stage push pull inverter.

Fig. 4 is the simple equivalent model of Fig. 3. V_A and Z_{in} are respectively the input voltage and impedance of three-stage cascade push pull inverter.

According to Kirchhoff's current law

$$\frac{V_A - V_{\text{out}}}{R_f} + \frac{V_A}{Z_{\text{in}}} = \frac{V_{\text{in}} - V_A}{Z_L} \tag{5}$$

$$\frac{V_{\text{in}} - V_A}{Z_L} + \frac{V_{\text{in}}}{1/sC_D} = I_S \tag{6}$$

$$V_{\text{out}} = A_{\text{total}} V_A \tag{7}$$

where Z_L is the impedance of inductor L. The transimpedance can be expressed as

$$Z_R = \left|\frac{V_{\text{out}}}{I_{\text{in}}}\right| = \left|\frac{A_{\text{total}} R_f}{(1+sC_D Z_L)\left[1 - A_{\text{total}} + R_f\left(\frac{1}{Z_{\text{in}}} + \frac{sC_D}{1+sC_D Z_L}\right)\right]}\right| \tag{8}$$

Bring $Z_{\text{in}} = 1/sC_{\text{in}}$ and $Z_L = Ls$ into the above equation, then

$$Z_R = \left|\frac{A_{\text{total}} R_f}{(1+s^2 C_D L)(1 - A_{\text{total}} + sC_{\text{in}} R_f) + sC_D R_f}\right| \tag{9}$$

Assuming that

$$\alpha = 1 + s^2 C_D L \tag{10}$$