Optik 125 (2014) 3315–3318

Contents lists available at ScienceDirect

Optik

journal homepage: www.elsevier.de/ijleo

High-speed CMOS readout integrated circuit for large-scale and high-resolution microbolometer array

Chao Fang[a,*], Xiqu Chen[a], Xinjian Yi[b,c]

[a] School of Electrical & Electronic Engineering, Wuhan Polytechnic University, Wuhan 430023, China
[b] Wuhan National Laboratory for Optoelectronics, Wuhan 430074, China
[c] State Key Laboratory for Imagine Processing and Intelligent Control, HUST, Wuhan 430074, China

ARTICLE INFO

Article history:
Received 3 July 2013
Accepted 18 December 2013

Keywords:
CMOS
ROIC
Microbolometer
FPA

ABSTRACT

A new CMOS readout integrated circuit (ROIC) for microbolometric focal plane array (FPA) is proposed in this paper. By applying multiple-module parallel working technique, the pixel readout speed of the CMOS ROIC can reach 10 MHz, which is very suitable for large-scale microbolometer array. The CMOS ROIC of each parallel working module consists of three major parts: direct injection (DI) input circuits, column-shared integrating circuits, and common noise-suppressing circuits. The readout structure of the ROIC is simple because of the DI input, shared and common circuits, and this makes the ROIC satisfy the requirements of small-pixel microbolometric FPA. Furthermore, the voltage signals from different working modules can be output according to a certain order through a high-speed output circuit. An experimental readout chip based on the proposed ROIC has been designed and fabricated to verify its readout function and performance. The measurement results of the experimental readout chip have successfully proved that the proposed CMOS ROIC can be applied to high-speed, low-noise, large-scale and high-resolution microbolometric FPA.

1. Introduction

In comparison with cooled FPA and pyroelectric uncooled FPA, microbolometric FPA has two chief advantages: one is that microbolometric FPA does not require liquid nitrogen cooling parts while cooled FPA requires [1–3], and the other is that microbolometric FPA works without mechanical chopper while pyroelectric uncooled FPA works with [4–6]. These two advantages make microbolometric FPA have excellent performance characteristics like low cost, small size and high stability. In recent 10 years, the performance of microbolometric FPA has made great progress with the improvement of fabricating processing for microbolometric arrays and the advance of integrated circuit technology for CMOS ROIC. Some key characteristic parameters as NETD (noise equivalent temperature difference) and sensitivity of modern microbolometric FPA are nearly close to those of cooled FPA, but there are still some requirements including high-speed, large-scale, high-resolution, and so on, for next-generation microbolometric FPA with the development of wide field of view and high-speed infrared image applications [7,8].

Conventional ROIC readout structures can meet some parts of the performance requirements for next-generation microbolometric FPA, while maybe degrading other parts of its performance characteristics. These simply-configured readout structures such as DI, source follower per detector (SFD), and gate-modulation input (GMI) are favourable for high-resolution and low-power-dissipation of microbolometric FPA, but their noise-level and stability are normally unacceptable for next-generation microbolometric FPA [9,10]. Other complex readout structures such as capacitor feedback transimpedance amplifier (CTIA) and feedback enhanced direct injection (FEDI) have low-noise and high-stability performance, but they are unfit for large-scale and high-resolution microbolometric FPA [11,12]. In our former experiments, we have designed and fabricated a kind of CMOS ROIC for uncooled FPA which achieves good readout performance in a small pixel size for high-resolution and low-noise [8,12].

In this paper, a new CMOS ROIC is proposed for next-generation microbolometric FPA. The CMOS ROIC can be divided into several parallel working modules, and each module has simply-constructional structure and high-noise-suppressing capability and suits low-noise and high-resolution microbolometric FPA. All these parallel working modules output their pixel-signals at same time row by row and column by column, and the infrared sensing voltage signals of the whole microbolometric FPA from different working modules can be output according to a certain order to form the video signal through a high-speed output circuit, which

* Corresponding author. Tel.: +8627 85504717; fax: +8627 85504715.
E-mail address: cxqdhlcly@sina.cn (C. Fang).

0030-4026/$ – see front matter © 2014 Elsevier GmbH. All rights reserved.
http://dx.doi.org/10.1016/j.ijleo.2013.12.057

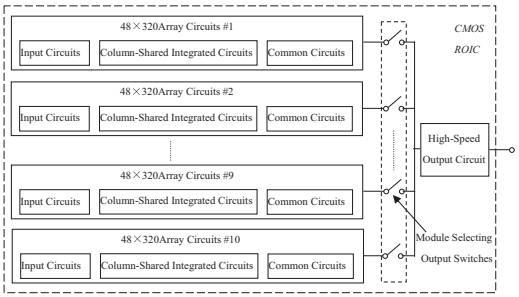

Fig. 1. The block diagram of 320 × 480 readout circuit structure.

indicates that the proposed CMOS ROIC also suits high-speed and large-scale microbolometric FPA.

2. The proposed CMOS ROIC structure

The proposed CMOS ROIC is composed of the input circuits, the column-shared integrated circuits, the common circuits, and the high-speed output circuit. This 480 × 320 ROIC structure is based on 48 × 320 array circuit architecture as shown in Fig. 1. The whole 480 × 320 CMOS ROIC is divided into 10 48 × 320 parallel working modules. It is worthwhile to note that all the columns in the whole CMOS ROIC are not orderly divided into 10 modules. The 48 columns in the module #1 are respectively corresponding to the columns 1, 11, 21, . . ., 461, 471 in the whole CMOS ROIC, other 48 columns in the module 2 are respectively corresponding to the columns 2, 12, 22, . . ., 462, 472 in the ROIC, and the last 48 columns in the module 10 are therefore respectively corresponding to these columns 10, 20, 30, . . ., 470, 480 in the same ROIC in a similar way. When the 480 × 320 CMOS ROIC works, the same row of these 10 modules are selected to output their voltage signals column by column simultaneously, and the output signals from different modules can be orderly output with these module selecting output switches to the high-speed output circuit in Fig. 1.

2.1. CMOS ROIC in module

Each module has 48 × 320 pixel input circuits of DI structure, 48 × 1 column-shared integrated circuits of CTIA, and a common noise-suppressing circuits of high correlated double sampling (HCDS). This CMOS ROIC schematic diagram is illustrated in Fig. 2. The basic operation of the CMOS ROIC can be briefly expressed as follows. The photon-generated current signals from a row of 48 × 1 DI input circuits are integrated and amplified by the row of 48 × 1 column-shared CTIA integration circuits, and then the integrated voltage signals of the integration circuits are processed column by column through the common HCDS noise-suppressing circuit to form a serial of high signal–noise ratio voltage output signals.

The detailed CMOS ROIC of each unit-cell in module is shown in Fig. 3, in which R_d is a microbolometer (when exposed to infrared light, its resistance can be changed) and R_b is the blind microbolometer (not exposed to infrared light). During the row selecting switch S_R is on, the column selecting switch S_C turns on at first and the reset switch S_{Reset} immediately turns on and the integration voltage of the column-shared CTIA integrated circuit is reset to the reference voltage V_{ref}. At time t after the column selecting switch S_C and the reset switch S_{Reset} turn off, the column selecting switch S_C turns on again with that N-MOS switch N_3 is on and the reversed photon-generated current integration voltage $\frac{1}{C_{\text{int}}}\int_0^t I_{\text{int}}dt$ and the reference voltage V_{ref} are sampled on the coupling capacitor C_c. At last, the reset switch S_{Reset} turns on again with that N-MOS switch N_3 turns off and the reference voltage V_{ref} is secondly sampled to the coupling capacitor, and the output voltage V_o

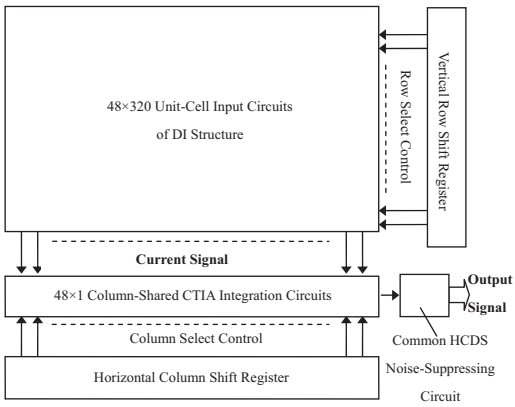

Fig. 2. Schematic diagram of the CMOS ROIC in module.

without consideration of the sampled noise is

$$V_o = (V_{ref} - V_{gsn}) - \left(V_{ref} - V_{gsn} - \frac{1}{C_{\text{int}}}\int_0^t I_{\text{int}}dt\right) = \frac{1}{C_{\text{int}}}\int_0^t I_{\text{int}}dt \quad (1)$$

where V_{gsn} is the voltage drop of the N-type source follower composed of the NMOS devices N_1 and N_2.

From Eq. (1), it can be found that the photon-generated current integration voltage is reversely output by the CMOS readout circuit. Additionally, the photon-generated current integration voltage is only sampled once and the noise from the CTIA integrated circuit and the N-type source follower composed of the NMOS devices N_1 and N_2 are sampled twice by the common HCDS noise-suppressing circuit during a row selecting time, so the common HCDS noise-suppressing circuit can effectively suppress correlated noise for that the sampling time interval between two noise-sampling times is approximately small to zero [8].

2.2. High-speed output circuit

In order to improve the pixel readout speed of the whole 480 × 320 ROIC, the CMOS ROIC in each module can work at its maximum output speed, which requires the high-speed output circuit in Fig. 1 has a very high maximum output speed for pixel signals. The designed high-speed output circuit in our laboratory is shown in Fig. 4. This CMOS output circuit mainly contains three stages: the pair of PMOS devices P_1 and P_2, the pair of NMOS devices N_4 and N_5, and the current source I_0 form a differential-input stage, the three NMOS devices N_6, N_7 and N_8 and two current sources I_1 and I_2 form a voltage amplifying stage, and the NMOS device N_9 and the current source I_3 form a voltage following stage to improve the output driving capability of the CMOS output circuit. The resistance R and capacitor C are adjustable to constitute a feedback channel, which can be used to elevate the output bandwidth and speed of the output circuit [13]. The resistance R_1 and R_f are utilized to

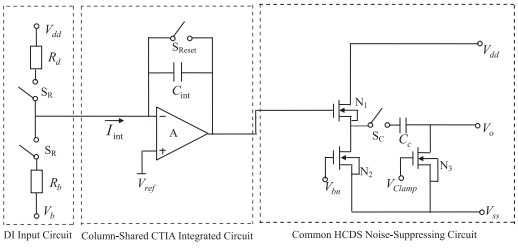

Fig. 3. The CMOS ROIC structure of each unit-cell in module.