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VSR5 optical transmission system and 12 × 10 Gbps VCSEL driver array design

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ABSTRACT

This paper introduces VSR (Very Short Reach) parallel optical interconnection in OC-768 applications, which is compliant with OIF (Optical Internetworking Forum) OIF-SFI5-01.0 and VSR5-01.0 agreements. A point to point experimental parallel transmission system is set up to convert 16 × 2.5 Gbps electrical signals to 12 × 3.318 Gbps optical signals, and vice versa. An OC-768 framer dichotomy search algorithm logic has been implemented in an converter IC, which greatly boosts up working speed and saves logic resources. In addition, a 12 × 10 Gbps VCSEL common cathode driver array has been fabricated by 0.18 μm CMOS technology. Tested by an OC-768 tester, a system bit error rate (BER) of lower than 1×10^{-12} has been obtained.

1. Introduction

With the rapid development in telecom technology, the demand for bandwidth is increasing rapidly. This paper describes a low-cost SONET/SDH OC-768 parallel optical link in VSR (very short reach) application. The VSR interface utilizes the 850 nm short wave VCSEL-based parallel optics technology.

To leverage this low cost technology in SONET/SDH OC-768 system, a deskew methodology is defined in OIF-SFI5-01.0 agreement [1] and a mapping and re-assembling of the OC-768 frame structure to 12 × 3.31875 Gbps parallel optical link configuration is defined in OIF VSR5-01.0 [2] respectively. An experimental system is designed to be compliant with the standards.

2. Functional overview

The OC-768 VSR is a bi-directional interface. As defined in OIF-VSR5-01.0 implementation agreement, receiver sensitivity shall be such that the BER $\leq 10^{-12}$ with the minimum optical power and other worst cases. A functional block diagram is illustrated in Fig. 1.

The SFI-5 (OC-768 SERDES Framer Interface) is an electrical interface between SONET framer and serializer/deserializer parts for OC-768 interfaces. An aggregate of 39.808 Gbps data rate is transferred by 16 × 2.488 Gbps data channels and a 2.488 Gbps deskew channel in duplex direction.

Because the skew and wander between data and clock can exceed a single bit period, no single clock samples all data channels simultaneously and hold times will be hardly achieved regarding skew, jitter and manufacturing tolerances. So a deskew channel (DSC) that contains a frame header and samples of data from the 16 data lanes is established to align these data channels.

The parallel optical interface is an MTP/MPO connector with 12 × 3.318 Gbps Multi Model Fiber (MMF) terminations in OIF VSR5-01.0 to transmit the OC-768 frame over very short distances. An FPGA performs the function of a converter and maps an SFI-5 data stream to 12 channels for output to parallel transmit optics in the transmit direction, and vice versa in the receive direction. The FPGA acts as a transparent converter without FEC (Forward Error Correction) or error correction functions as defined in a 12 channel parallel optics solution. The converter contains all the digital circuits for deskewing data in duplex directions, frame and byte alignment as well as the analog circuitry required for clock and data recovery (CDR) and MUX/DEMUX.

3. VSR5-1 system

3.1. Converter

The basic function of the converter in the VSR link is shown in the functional block diagram of Fig. 2.

In the TX direction, the converter receives 16 × 2.488 Gbps data and a deskew (TXDSC) signal from an OC-768 pattern generator. The converter firstly performs clock and data recovery from each channel, then 1:16 demuxes 17 channels to deskew logic. Then, the deskew logic eliminates skews between the 16 data lanes using information contained in the DSC channel. The OC-768 framer locates A1A2 delimiter in OC-768 data frames and performs basic word alignment. Finally, the framed data are mapped to 12 chan-

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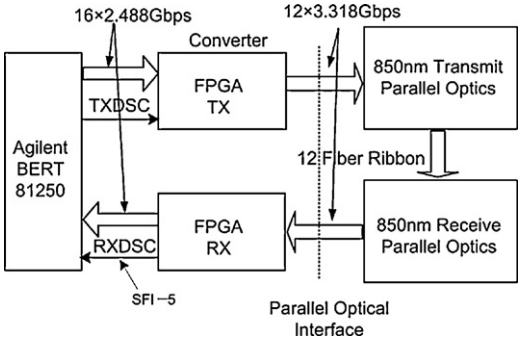

Fig. 1. Functional block diagram of OC-768 VSR5 interface.

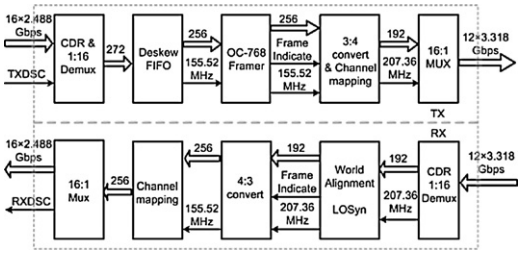

Fig. 2. VSR5-01.0 block diagram.

nels, whose output is coupled to a self-made 850 nm transmission module.

In the RX direction, the converter receives 12×3.318 Gbps signals from a commercial parallel optical module (PARACER PR2000Rx). The received portion of the SERDES performs clock and data recovery (CDR) and 1:16 demux from each channel. The converter aligns individual channels by each channel frame delimiters to compensate for any inter-channel skew that may occur due to propagation delay between these channels. Then, the converter reassembles the 12 channels of data into 16×2.488 Gbps and a deskew (RXDSC) SFI-5 signal and re-maps the OC-768 framing bytes.

3.1.1. SFI-5 deskew

The function of the deskew logic is to recognize the framing and header bytes in the TXDSC channel, to identify the start of the reference data that is replicated from each of TXDATA channel. As illustrated in Fig. 3, the TXDSC frame is generated in the source device, consisting of 4 framing bytes (A1A1A2A2), 4 bytes of expansion header (E1–E4) and 128 bytes of data samples. The data samples are duplicated from the TXDATA[15:0] in 8-byte sets, starting with TXDATA[15] and ending with TXDATA[0].

Fig. 4 shows SFI-5 deskew logic. After frame delimiters are found from TXDSC channel, each of the TXDATA channels is then compared with the TXDSC channel in turn. The deskew logic performs a pattern match between the replicated data in TXDSC with the original data in the corresponding TXDATA[X] lane.

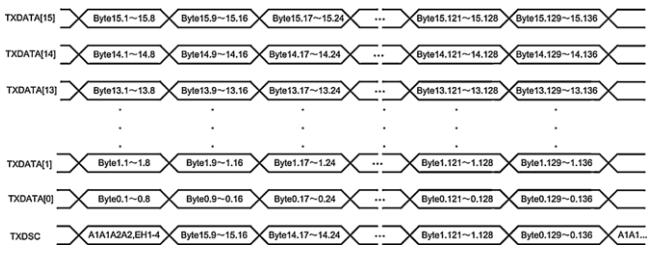

Fig. 3. TXDSC functional timing.

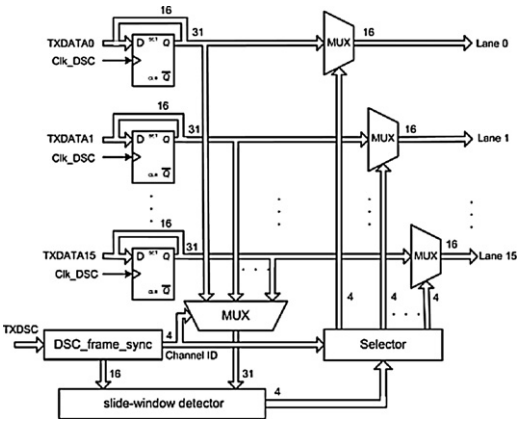

Fig. 4. SFI-5 deskew logic.

Where there is a match, the skews between TXDATA and TXDSC is found. According to SFI-5 agreements, 11 unit intervals (UI) of wander is allowed including mechanical and routing mismatches in 16 data lanes, as well as temperature and power changes and so on.

The deskew logic runs at a low speed of 155.52 MHz, so it is suitable to be implemented in FPGA. Another approach is that the working speed is 312.5 MHz and FIFO control logic is adopted [3,4]. Reference [5] uses a 7-bit shift register and a 64-bit compare window. Compared with the method, our approach consumes lower power supply and simplifies FIFO control logic. Therefore, a 1:16 demultiplexer is needed in every data lane. It receives 17 lanes (16 data and DSC) of 2.5 Gbps data on 16 bit wide 155.52 Mbps buses. Each lane's data have arbitrary bit position within the 16-bit bus.

Firstly, the DSC_frame_sync logic aligns the TXDSC data at byte boundaries by delimiter A1A1A2A2 and generates a channel ID signal. Meanwhile, each incoming 16-bit TXDATA is combined with the lower 15 bits of the data word from the previous cycle, and fed into a 16-port MUX module. Then, the data enter a slide-window detector, which will generate a 4-bit signal that indicates each lane skew position from 0 to 15-bit. Finally, the selector and output MUX will select the deskewed data according to channel ID and skew position in each channel, so that the output data can be precisely aligned on the byte boundary.

Moreover, the SFI-5 deskew logic serves two purposes: (1) to transfer all 17 data lanes which have individual clocks to a common master clock derived from 155.520 MHz clock generated by CDR and (2) to absorb any wander in the data lanes with respect to each other or to the common transmit clock. The deskew logic can compensate for 11 bits of static skew and 21 bits of dynamic wander/jitter, which meets OIF agreements.

3.1.2. OC-768 framer

OC-768 framer exams the A1A2 transition in the incoming data. Once a transition is found, the data words can be shifted in time corresponding to the byte boundaries of the incoming data. In this application, the 16×2.488 Gbps deskewed SFI-5 data stream is 1:16 demuxed into frame alignment logic, which equals to demux the OC-768 data stream by 1:256 ratio. So, the A1A2 boundary will be arbitrary in any 1/256 position of the incoming data frame.

Conventional framing approaches operate in serial or parallel manner to search frame synchronous code (FSC) A1A2 [6–9]. However, with the increment of data bus width, these strategies impose strict timing constraint on the related logic circuits, and in turn, lead to substantial increasing in the frame search logic design complexity.

If 768 A1 in an OC-768 data stream are divided into data groups by each 256 bit width, there are at least 23 same data segments (24