Optik 127 (2016) 4669–4674

Contents lists available at ScienceDirect

Optik

journal homepage: www.elsevier.de/ijleo

Design and simulation of linear logic gates in the two-dimensional square-lattice photonic crystals

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ARTICLE INFO

Article history:
Received 4 January 2016
Accepted 8 February 2016

Keywords:
All-optical logic gates
Coupled-mode theory
Finite-difference time-domain
Photonic crystal
T-branch combiner

ABSTRACT

We have proposed all-optical three-port AND, OR, XOR and NOT photonic crystal logic gates, based on modified symmetric T-branch combiners. Using the temporal coupled-mode theory the operation of the symmetric T-branch combiner has been investigated and the conditions which lead to a maximum power at the output port have been obtained. At the output port of the proposed devices, the logics 1 and 0 are defined as a more than 42% and a less than 14% of the transmission, respectively. The minimum intensity contrast ratio of the suggested logic gates is about 4.77 dB. The operations of the proposed devices are examined using time-domain transition-response simulations which have been performed using two dimensional finite-difference time-domain method.

1. Introduction

The rapidly growing use of all-optical processing systems, calls for ultra-compact and fast all-optical logic gates. The used designs for the creation of these devices can be basically classified into two categories: nonlinear and linear designs. The nonlinear designs are based on fiber gratings [1,2], semiconductor optical amplifiers (SOAs) [3], semiconductor microresonators [4], periodically poled lithium niobate (PPLN) waveguides [5–8], and so on. Unfortunately, most of these designs suffer from definite limitations such as large sizes, low speed operations, high drive-powers, or complex integrations. The linear designs are based on the self-collimation effect [9], multi-mode interference effect [10] and light beam interference effect [11,12]. The other candidate for all-optical logic gates are the photonic crystal (PC) based devices which can used in both the linear and the nonlinear regimes. There have recently been proposed several nonlinear designs of optical logic gates in two-dimensional (2D) PCs [13–16], but due to relatively small Kerr coefficient of the conventional nonlinear materials, there is still a great need to high optical drive-powers. In linear regime, and using the accurately controlled optical path difference in PC waveguides, realization of fast, low power and high contrast ratio all-optical logic gates are possible [12,17]. In this paper, we present an analytical approach for designing of different linear logic gates in PCs with square lattice. The coupled-mode theory (CMT) is employed to analyze the behavior of the proposed all-optical three-port AND, OR, XOR and NOT logic gates. The validity of the proposed logic gates is investigated using 2D finite-difference time-domain (FDTD) method. The simulation results verify the validity of the proposed design approaches.

2. Model and operating principles of the proposed three-port OR, AND, XOR and NOT logic gates

All of our presented logic gate designs are composed of a typical symmetric T-branch combiner, which will be slightly modified for designing different types of logic gates. First, we evaluate the operation of a typical symmetric T-branch combiner that its CMT based schematic diagram is shown in Fig. 1. As can be seen, S_{+i} and S_{-i}, where $i = 1, 2$ and 3, represent the incoming and outgoing electromagnetic (EM) waves into the PC resonator, respectively. The CMT equations that describe the temporal change of the normalized mode amplitude of the resonator, a, are described by [18]

$$\frac{da}{dt} = j\omega_0 a - a\sum_i \frac{1}{\tau_i} + \sum_i \left(S_{+i}\sqrt{\frac{2}{\tau_i}} \right), \quad (1)$$

$$S_{-i} = S_{+i} + \sqrt{\frac{2}{\tau_i}}a, \quad (2)$$

where $1/\tau_1$, $1/\tau_2$ and $1/\tau_3$ are the decay rates of the resonant cavity into the port 1, 2 and 3, respectively. When the EM wave is

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http://dx.doi.org/10.1016/j.ijleo.2016.02.012
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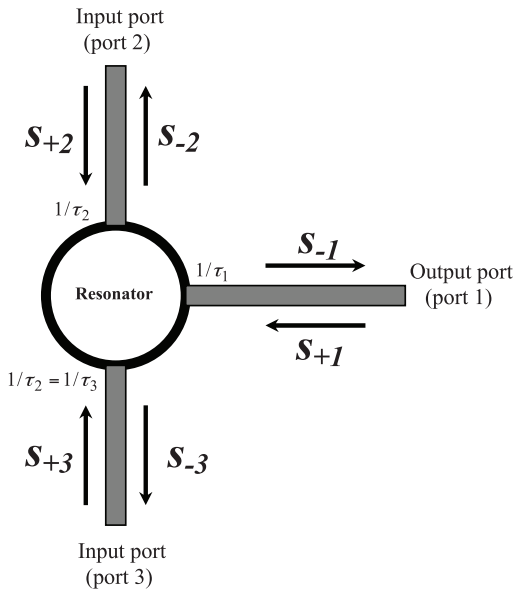

Fig. 1. The CMT based schematic diagram of a T-branch combiner.

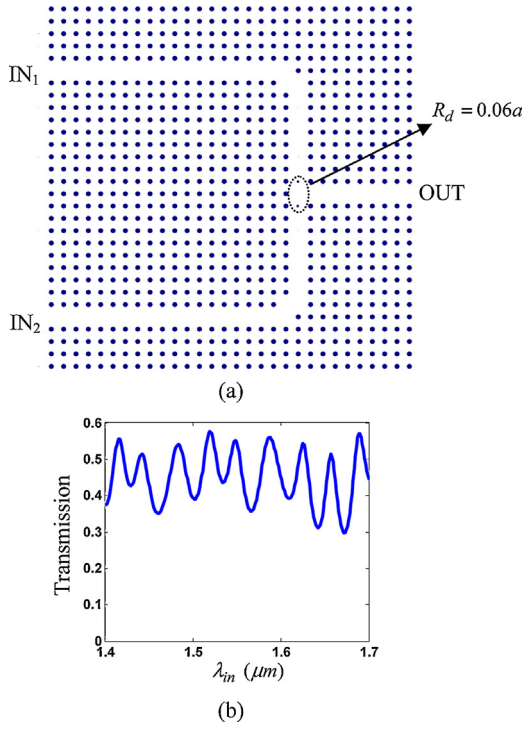

Fig. 2. (a) The schematic structure of the proposed PC OR logic gate. (b) The transmission spectrum at the OUT port.

launched only from the upside into the resonator $(S_{+1}, S_{+3} = 0)$, and assuming that $1/\tau_2 = 1/\tau_3$ and $\omega = \omega_0$, one can find

$$T_1 = \left|\frac{S_{-1}}{S_{+2}}\right|^2 = \frac{\left(4/\tau_1\tau_2\right)}{\left(\left(1/\tau_1\right) + \left(2/\tau_2\right)\right)^2} = \frac{4\kappa}{(1+2\kappa)^2}, \tag{3}$$

$$T_3 = \left|\frac{S_{-3}}{S_{+2}}\right|^2 = \frac{\left(2/\tau_2\right)^2}{\left(\left(1/\tau_1\right) + \left(2/\tau_2\right)\right)^2} = \frac{4\kappa^2}{(1+2\kappa)^2}, \tag{4}$$

Table 1
The operation of OR gate. Inputs: $(p_{in} : 0) \equiv$ state 0, $(p_{in} : 0.5P_0) \equiv$ state1, Output: $\left(p_{out}/p_{in} \le 0.14\right) \equiv$ state 0, $\left(p_{out}/p_{in} \ge 0.42\right) \equiv$ state1.

IN_2	IN_1	Transmission (%)	Logic output
0	0	0	0
0	1	50	1
1	0	50	1
1	1	200	1

4.77 dB ≤ ICR.

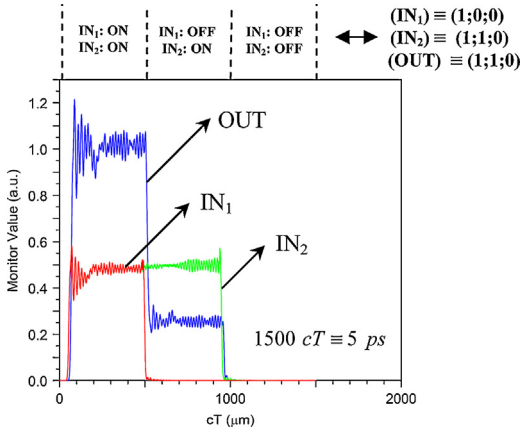

Fig. 3. The time-domain transition-response of the proposed OR logic gate.

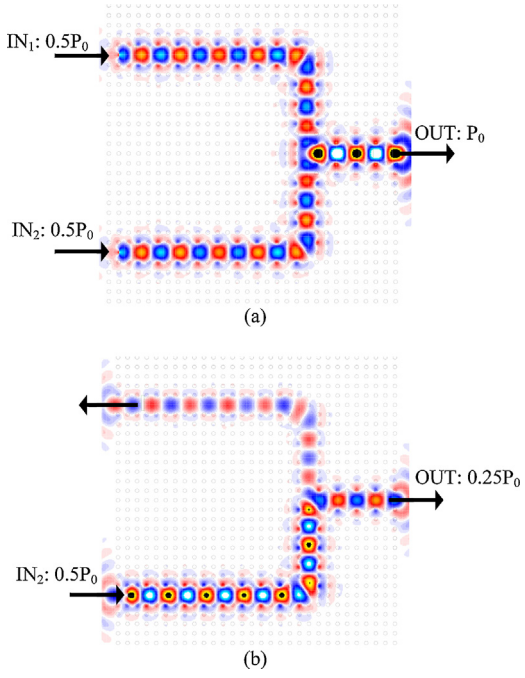

Fig. 4. The field distributions of the proposed OR logic gate when (a) $(IN_1, IN_2) \equiv (1,1)$. (b) $(IN_1, IN_2) \equiv (0,1)$.

$$R = \left|\frac{S_{-2}}{S_{+2}}\right|^2 = \frac{\left(1/\tau_1\right)^2}{\left(\left(1/\tau_1\right) + \left(2/\tau_2\right)\right)^2} = \frac{1}{(1+2\kappa)^2}, \tag{5}$$

where $\kappa = \tau_1/\tau_2$. From Fig. 1 and using of Eq. (3), one can find that the maximum transmission power coefficient of 50% into the output port (port 1) can be achieved when $\kappa = 1/2$. This condition can be easily satisfied through a reduction in the decay rates of the resonant cavity into the vertical branches in Fig. 1. Furthermore, in this case one can see that $T_3 = R = 25\%$. Accordingly, in the best case,