Optik 125 (2014) 6183–6188

Contents lists available at ScienceDirect

Optik

journal homepage: www.elsevier.de/ijleo

Frequency encoded optical four-bit adder/subtractor with control input using semiconductor optical amplifiers

Kousik Mukherjee

Department of Physics (UG & PG), B.B. College, Asansol, West Bengal, India

ARTICLE INFO

Article history:
Received 6 July 2013
Accepted 4 June 2014

Keywords:
Semiconductor optical amplifier
Optical computation
Four wave mixing
Frequency encoding

ABSTRACT

Optical adder/subtractor for two four-bit frequency encoded binary numbers are proposed and designed based on four wave mixing, add drop multiplexing and frequency conversion in semiconductor optical amplifier. The input bits and the control input are intensity-modulated signal of two specific frequencies suitable for optical communication in the C band of wavelength. The device can distinguish negative and positive results and controlled operation are most promising in this proposal. The use of semiconductor optical amplifiers along with frequency encoding makes the system very fast and useful for future optical communication and computation systems.

1. Introduction

The demand of high speed processing of huge data is possible only in optical domain because the speed of electronic processors has almost reached the saturation. The basic element of an optical logic processor is the optical switch. An optical switch works on the principles of intensity switching [1–5], polarization switching [6–8], phase switching [9,10] or frequency switching [11–22]. Frequency is a fundamental property of light, it does not alter during propagation but can be changed by non-linear properties of different materials and devices. So the technique of frequency switching has become popular among researchers in present days [11–22]. In frequency switching technique, the states of information are represented by signal of different frequencies [23–25]. This is called frequency encoding of states. In the work by Jorgensen [23], three different frequencies of the primary light signals blue, red and green are used to represent the states of information. In the work by Hill et al. [24,25], the complementary states of information are represented by two different wavelengths. One of the most important device for implementing optical devices is semiconductor optical amplifier (SOA) which shows different types of non-linearity like cross gain modulation (XGM), cross phase modulation (XPM), four wave mixing (FWM), etc. [26,27]. SOA is also important because of its high-speed capability, low noise, less operating power and integration ability and is very popular in present day optical computation and communication research.

Full adder and full subtractor are basic building block for optical logic processors for computation and communication systems in future. In last decade, a few proposals have been found on these devices [28–31]. Most of these are using intensity encoding and proposals based on frequency encoding are very few [15,32,21]. Frequency encoded simultaneous adder–subtractor is least in number [15], which is based on polarization rotation based switching along with add drop multiplexer (ADM) and is complex in hardware. In this communication, SOA based four wave mixing (FWM) is used for the implementation of the adder/subtractor unit. The unit can be used as adder and subtractor by using a control input, which is also frequency-encoded signal. When the control input is low, the unit works as an adder and when the control is high, the unit subtract in two's complement format.

2. Basic building blocks and working principles of the adder/subtractor unit

In digital electronics it is well known that two four bit numbers can be added using four full adders and the two's complement of any four bit number is found by flipping each bits of the number i.e. one's complement and then adding '1' to the one's complement of the number. So to achieve two's complement in controlled way we have to use X-OR gates and full adders. For the implementation of the full adders AND, OR and X-OR logic gates are required. So the basic building blocks for the implementation of the proposed optical four bit two's complement adder/subtractor unit is OR, AND, and X-OR gates only. All the logic gates used in this communication are frequency encoded all optical logic gates based on ADM, FWM in SOA and frequency conversion in reflective semiconductor optical

E-mail address: lipton007@rediffmail.com

http://dx.doi.org/10.1016/j.ijleo.2014.06.041
0030-4026/

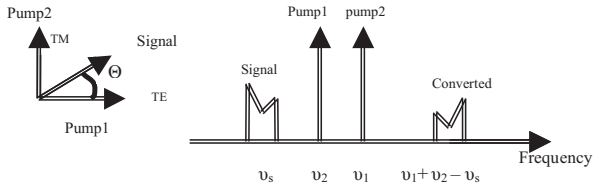

Fig. 1. Polarization independent four wave mixing.

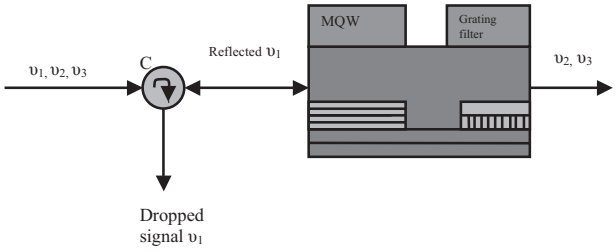

Fig. 2. Tunable SOA filter ADD/DROP multiplexer.

amplifiers (RSOA). Based on these mechanisms in SOA, all optical frequency encoded logic gates [12] and full adder [32] was already proposed. The FWM used to implement the logic gates and devices is polarization independent dual pump configuration with orthogonal polarization of the pump signals [33] is shown in Fig. 1. The two pumps interact with the input data signal in the SOA and generate a new conjugate signal at another frequency. This newly generated frequency is multiplexed and converted to get different output at two different frequencies as required by the frequency encoding and different logic gates are implemented. The frequency multiplexing is done by the add drop multiplexer (Fig. 2) as described in [34]. The frequency conversion to get the desired output of the gates is done by reflective semiconductor optical amplifier (Fig. 3) based on the principle described in [35].

2.1. Logic gates and the full adder for the implementation of the adder/subtractor

The logic gates used in this communication are described in details in the work [12]. The NOT gate is the modified NOR gate which is achieved by making two inputs of the NOR gate same. In frequency encoding the low (0) state is represented by a signal of frequency ν_1 and high (1) state is represented by another signal of frequency ν_2. This type of encoding has several advantages compared to other conventional encoding systems [11–25,32]. The working of the gates is described below very in short.

2.1.1. NOT gate

When A is a signal of frequency ν_1 (low) the FWM generated output is a signal of frequency $2\nu_1-\nu_s$ and is converted to a signal of frequency ν_2 by RSOA 1 in Fig. 4. Similarly when A is a signal of frequency ν_2 (high) the FWM generated output is a signal of frequency $2\nu_2-\nu_s$ and is converted to a signal of frequency ν_1 by RSOA 2. So the unit in Fig. 4 works like a NOT gate.

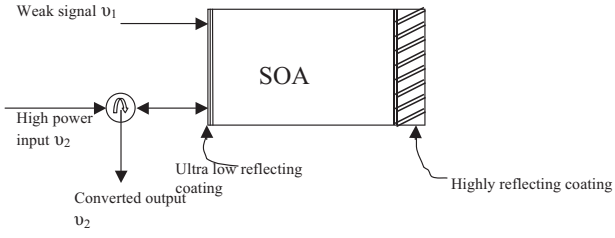

Fig. 3. Reflective SOA.

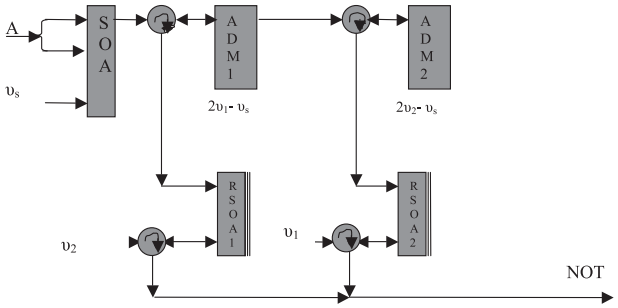

Fig. 4. Frequency encoded NOT gate.

Table 1
Truth table of the logic gates OR, AND and X-OR gate.

A	B	OR	AND	X-OR
$\nu_{1(0)}$	$\nu_{1(0)}$	$\nu_{1(0)}$	$\nu_{1(0)}$	$\nu_{1(0)}$
$\nu_{1(0)}$	$\nu_{2(1)}$	$\nu_{2(1)}$	$\nu_{1(0)}$	$\nu_{2(1)}$
$\nu_{2(1)}$	$\nu_{1(0)}$	$\nu_{2(1)}$	$\nu_{1(0)}$	$\nu_{2(1)}$
$\nu_{2(1)}$	$\nu_{2(1)}$	$\nu_{2(1)}$	$\nu_{2(1)}$	$\nu_{1(0)}$

2.1.2. OR gate

When any one of the inputs A and B is a signal of frequency ν_2, the output is a signal of frequency ν_2 i.e. high. If both the inputs are signals of frequency ν_1, the output is a signal of frequency ν_1 (low).

2.1.3. AND gate

When any one of the inputs A and B is a signal of frequency ν_1, the output is a signal of frequency ν_1 (high). If both the inputs are signals of frequency ν_2, the output is a signal of frequency ν_2 (high).

2.1.4. X-OR gate

When A and B is signals of different frequencies, the output is high. If they are of it output is low.

The truth table of the logic gates is shown in Table 1. The working of the full adder is described in Table 2. The implementation of the full adder for two 2-bit numbers is described in [32].

3. Implementation of the adder/subtractor unit and the algorithm of the operation

Using the logic gates and full adder described in Section 2.1 of this communication an adder–subtractor unit can be easily designed as shown in Fig. 5. The first stage is an array of four X-OR gate are used to flip each bits of a four bit number in a controlled way depending on the control input C, the second stage is an array of four single bit full adder. The first two stages are used to generate result of operation of the addition and subtraction depending on

Table 2
Operating conditions and outputs of the full adder.

Inputs			Outputs	
A_n	B_n	C_{n-1}	Sum	Carry
ν_1	ν_1	ν_1	ν_1	ν_1
ν_1	ν_1	ν_2	ν_2	ν_1
ν_1	ν_2	ν_1	ν_2	ν_1
ν_1	ν_2	ν_2	ν_1	ν_2
ν_2	ν_1	ν_1	ν_2	ν_1
ν_2	ν_1	ν_2	ν_1	ν_2
ν_2	ν_2	ν_1	ν_1	ν_2
ν_2	ν_2	ν_2	ν_2	ν_2