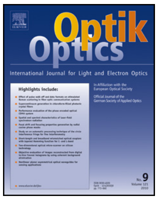
Optik 125 (2014) 6227–6230

Contents lists available at ScienceDirect

Optik

journal homepage: www.elsevier.de/ijleo



# Current-mode current-tunable four-phase quadrature oscillator

Shiqiang Chen[a,b,*], Junfeng Wang[b]

[a] College of Computer Science, Sichuan University, Chengdu, PR China
[b] Hubei University for Nationalities, Enshi, PR China

ARTICLE INFO

*Article history:*
Received 8 November 2013
Accepted 6 June 2014

*Keywords:*
Circuit
Current mode
Current differencing transconductance amplifiers
Quadrature oscillator

ABSTRACT

A current-mode current-tunable four-phase quadrature oscillator (QO) using current differencing transconductance amplifiers (CDTA) is presented in this paper. The proposed QO consists of three CDTAs and two grounded capacitors, which can provide four quadrature current outputs at high impedance nodes. The proposed QO has the advantages of electronically and independently control of oscillation condition and oscillation frequency. Moreover, the active and passive sensitivities of the QO are low. Cadence IC Design Tools 5.1.41 post-layout simulation results are included to confirm the theory.

## 1. Introduction

As the current-mode circuits have the advantages of low power consumption, inherently wide bandwidth and larger dynamic range, they have received considerable attention [1]. The current differencing transconductance amplifier (CDTA) is a recently introduced current mode building block by Biolek in 2003 [2]. It is a really current-mode element whose input and output are current form, and it is widely used in designing active filters [3–8], current limiters [9], oscillators [10] and many other analog signal processing circuits.

The CDTA-based quadrature oscillators are reported in Refs. [11–19]. However, the works in Refs. [11–18] cannot provide electronically controlled CO and FO, which cannot be used as variable frequency oscillator; the works in Refs. [11,12,16] suffer from floating capacitors, and the work in Refs. [11–14,17,18] use resistors, and they are not suitable for monolithic integration; the BJT technology is used in Ref. [19], and it is not compatible with the CMOS digital integrated circuit to realize monolithically integration.

In this paper, a new CDTA-based current-mode four-phase QO with three CDTAs and two grounded capacitors is presented. The attractive advantage of the proposed QO is the condition of oscillation (CO) and frequency of oscillation (FO) of the quadrature oscillator can be adjusted electronically and independently by a bias voltage, and it is suitable for variable frequency oscillator (VFO). Moreover, the proposed QO is completely resistor-less, and it can provide four quadrature outputs at high impedance nodes. The performance of the proposed QO is demonstrated by Cadence IC Design Tools 5.1.41 post-layout simulation results.

## 2. Theory and principle

### 2.1. *Current differencing transconductance amplifiers*

Fig. 1a shows the symbol of CDTA, and Fig. 1b is the equivalent circuit of the CDTA. The terminal relations of the CDTA can be characterized by the following set of equations [4]:

$$\begin{cases} v_p = v_n = 0 \\ i_z = i_p - i_n \\ i_x + = g_m v_z = g_m Z_Z i_Z \\ i_x - = -g_m v_z = -g_m Z_Z i_Z \end{cases} \tag{1}$$

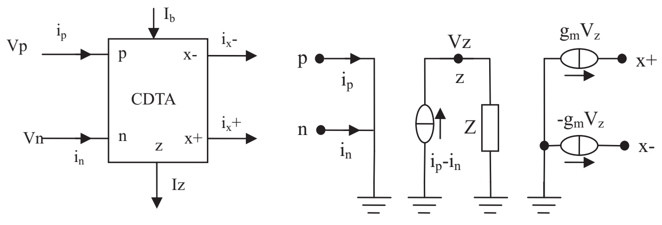
In Fig. 1, p and n are the input terminals, z and x are the output terminals, $g_m$ is the transconductance gain, and Zz is the external impedance connected to the terminal Z. From Eq. (1), the current $i_z$ is the difference of the currents at p and n ($i_p - i_n$), and it flows from the terminal z into the impedance Zz. The voltage at the terminal z is transferred to a current at the terminal x ($i_x$) by a transconductance gain ($g_m$), which can be electronically controlled by an external bias current $I_b$.

The CDTA used in this work is shown in Fig. 2.

---

* Corresponding author at: College of Computer Science, Sichuan University, Chengdu, PR China.
*E-mail address:* 124900808@qq.com (S. Chen).

http://dx.doi.org/10.1016/j.ijleo.2014.06.142
0030-4026/© 2014 Elsevier GmbH. All rights reserved.



(a) Symbol for the CDTA (b) Ideal model of the CDTA

**Fig. 1.** Symbol and ideal model of CDTA.

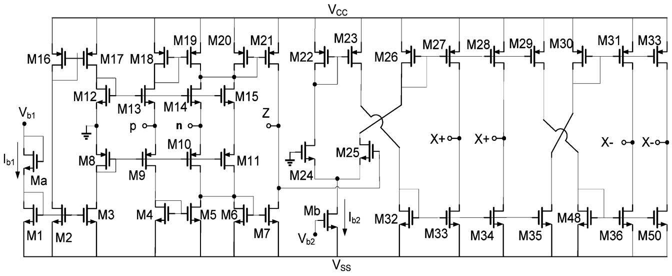


**Fig. 2.** CMOS-based CDTA in this work [15].

### 2.2. The proposed current mode quadrature oscillator

Fig. 3 is the proposed four-phase quadrature oscillator, which employs three CDTAs and two grounded capacitors. The grounded capacitors used in the QO are effective to eliminate various of parasitic capacitance.

A routine circuit analysis using Eq. (1), we can get the characteristic equation of the QO is:

$$s^2C_1C_2 + s(g_{m2} - g_{m1})C_2 + g_{m2}g_{m3} = 0 \tag{2}$$

where $g_{m1}$, $g_{m2}$ and $g_{m3}$ are the transconductance of the CDTA$_1$, CDTA$_2$ and CDTA$_3$, respectively.

From Eq. (2), the CO and FO of the QO can be expressed as:

$$g_{m2} = g_{m1} \tag{3}$$

$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}} \tag{4}$$

From Eqs. (3) and (4), it can be seen that the CO can be adjusted independently by the transconductance $g_{m1}$ without disturbing the FO; the FO can be tuned independently by the transconductance $g_{m3}$ without disturbing the CO.

From Fig. 3, the current transfer function between $i_{o1}$ and $i_{o2}$ is:

$$\frac{i_{o1}(s)}{i_{o2}(s)} = \frac{g_{m2}}{sC_2} = \frac{i_{o1}(j\omega)}{i_{o2}(j\omega)} = \frac{g_{m2}}{\omega C_2}e^{-j90^\circ} \tag{5}$$

So, the phase difference between $i_{o1}$ and $i_{o2}$ is 90°, and the two currents are quadrature.

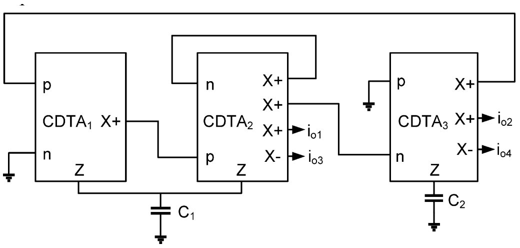


**Fig. 3.** The proposed current-mode QO.

Because the CDTA can provide multiple outputs, and another two inverted output currents $i_{o3}$ and $i_{o4}$ can be obtained easily. Thus, the relations of all the output currents can be expressed as:

$$\begin{cases} i_{o1} = -i_{o3} \\ i_{o2} = -i_{o4} \end{cases} \tag{6}$$

From Eqs. (5) and (6), it is clear that the proposed QO can provide four quadrature current outputs.

## 3. Non-ideal analysis

Taking the tracking errors of the CDTA into account, the port relations of the non-ideal CDTA can be rewritten as:

$$\begin{cases} v_p = v_n = 0 \\ i_z = \alpha_p i_p - \alpha_n i_n \\ i_x+ = \beta g_m v_z \end{cases} \tag{7}$$

where $\alpha_p = 1 - \varepsilon_p$ denotes the current tracking error from terminal p to z, $\alpha_n = 1 - \varepsilon_n$ denotes the current tracking error from terminal n to z, and $\beta$ is transconductance inaccuracy factor from the z to x terminals of the CDTA, respectively.

Taking the non-idealities in Eq. (7) into account, the non-ideal characteristic equation of the QO can be expressed as:

$$s^2C_1C_2 + s(\alpha_{n2}\beta_2 g_{m2} - \alpha_{p2}\beta_1 g_{m1})C_2 + \alpha_{p1}\alpha_{n3}\beta_2\beta_3 g_{m2}g_{m3} = 0 \tag{8}$$

The CO and FO of the proposed QO get modified and are given as:

$$\alpha_{n2}\beta_2 g_{m2} = \alpha_{p2}\beta_1 g_{m1} \tag{9}$$

$$\omega_o = \sqrt{\frac{\alpha_{p1}\alpha_{n3}\beta_2\beta_3 g_{m2}g_{m3}}{C_1C_2}} \tag{10}$$

where $\alpha_{pi}$, $\alpha_{ni}$ and $\beta_i$ are the parameters $\alpha_p$, $\alpha_n$ and $\beta$ of the $i$-th CDTA, respectively.

It can be seen from Eqs. (9) and (10) that if the tracking errors of CDTA$_1$ and CDTA$_2$ are equal, the CO of the proposed QO will not be affected; however, the FO of the QO will deviate from the ideal value, because of the tracking errors. In this case, the deviation of the FO can be compensated by trimming the transconductance $g_{m3}$.

From Eq. (10), the active and passive sensitivities of $\omega_o$ are low, and they can be expressed as:

$$\begin{cases} S^{\omega_o}_{g_{m2},g_{m3},\alpha_{p1},\alpha_{n3},\beta_2,\beta_3} = \frac{1}{2} \\ S^{\omega_o}_{g_{m1},\alpha_{n1},\alpha_{p2},\alpha_{n2},\alpha_{p3},\beta_1} = 0 \\ S^{\omega_o}_{C_1,C_2} = -\frac{1}{2} \end{cases} \tag{11}$$

## 4. Post-layout simulation results

The proposed QO is verified using Cadence IC Design Tools 5.1.41 Spectre simulator with standard Charted 0.18 μm CMOS technology. The chip layout design strictly obeys the Chartered Design Rule (YI-093-DR001_Rev1V_1.8V-3.3V) and Chartered Spice Model spec(yi093dr001_1v_00_20090731a), and it is designed as symmetrically as possible to minimize the mismatch in the signal paths. In the post-layout simulation, the supply voltage is ±1.2 V, the bias voltages $V_{b2} = -0.7$ V, the capacitors $C_1 = 8$ pF, $C_2 = 19$ pF.

Fig. 4 is the simulated $V_{o1}$, $V_{o2}$, $V_{o3}$ and $V_{o4}$ during initial state with 500 Ω load resistors, and it is clear that the starting time of the proposed QO is about 0.25 μs; Fig. 5 is the simulated quadrature outputs $V_{o1}$, $V_{o2}$, $V_{o3}$ and $V_{o4}$ from 0.5 μs to 0.525 μs with 500 Ω load resistors.