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Circuit designs of ultra-fast all-optical modified signed-digit adders using semiconductor optical amplifier and Mach–Zehnder interferometer

Abdallah K. Cherri*, Ayman S. Al-Zayed

Kuwait University, College of Engineering and Petroleum, Department of Electrical Engineering, P.O. Box 5969, Safat 13060, Kuwait

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Abstract

The need for increasingly high-speed digital optical systems and optical processors demands ultra-fast all-optical logic and arithmetic units. In this paper, we combine the attractive and powerful parallelism property of the modified signed-digit (MSD) number representation with the ultra-fast all-optical switching property of the semiconductor optical amplifier and Mach–Zehnder interferometer (SOA–MZI) to design and implement all-optical MSD adder/subtracter circuits. Non-minimized and minimized techniques are presented to design and realize efficient circuits to perform arithmetic operations. Several all-optical circuits' designs are proposed with the objective to minimize the number of the SOA–MZI switches, the time delay units in the adders, and other optical elements. To use the switching property of the SOA–MZI structure, two bits per digit binary encoding for each of the trinary MSD digits are used. The proposed optical circuits will be very helpful in developing hardware modules for optical digital computing processors.

Keywords: Optical computing; MSD numbers; All-optical gates; Semiconductor optical amplifier; Mach–Zehnder interferometer

1. Introduction

Parallel processing and high speed are two of the most important features required to enhance the overall performance of today's computers [1,2]. In electronics computing, the processing speed is limited by the inherent sequential processing as well as by the generation/propagation of carry bits in arithmetic operations. Due to inherent parallelism of optics, optoelectronics computing seems to offer an attractive solution to overcome the limitation of the sequential processing, by exploiting some of the excellent features of optics such as the high-speed computation, high temporal/spatial bandwidth, and non-interfering communications. The second limitation of the operational speed of electronics computing is the use of the binary number system where long carry/borrow bit propagation paths exist during the arithmetic operations. This limitation motivates researchers to look for alternative non-binary number systems [3–11] for designing high-speed arithmetic units. Among the alternatives, the redundant signed-digit number system [12–20] offers fast arithmetic operations due to its carry-free propagation property. Another important property of signed-digit number is that both positive and negative digits are allowed in the same representation. Signed-digit number

*Corresponding author. Tel.: +965 2498 7376; fax: +965 2498 7451.
E-mail addresses: cherri@eng.kuniv.edu.kw (A.K. Cherri), alzayed@eng.kuniv.edu.kw (A.S. Al-Zayed).

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system is being extensively explored in optics [11–20], for use in reliable designs and high-speed addition, subtraction, multiplication, division, and square root algorithms. The redundancy provided in signed-digit representation allows for fast addition/subtraction because the sum/difference digit is a function of only the digits in two adjacent digit positions for radix greater than 2, and three adjacent digit positions for a radix of 2 (the modified signed-digit number (MSD)). Thus, the add time for two redundant signed-digit numbers is constant and independent of the word length of the operands, which is the key to high-speed computation.

On the other hand, and for last three decades, there has been a desire to use optics to realize all-optical computing using digital optical elements. Nowadays, ultra-fast and all-optical processors are becoming very demanding in the high-capacity core networks to avoid optoelectronics conversions. To accommodate high data rates, one needs to avoid or eliminate the need to convert the optical signals to electronics signals and back to optical signals [21–25]. Recently, the development of different ultra-fast and all-optical switches has received considerable interest allover the world for future optical computing and optical information processing [21–25]. Nonlinear optical material provides the major support to optical switching, which is the base of all-optical logic and algebraic processing. For instance, schemes such as nonlinear optical loop mirror (NLOM), terahertz optical asymmetric demultiplexing (TOAD), semiconductor optical amplifier (SOA) waveguide based on a Michelson interferometer (MI), ultra-fast nonlinear interferometric and interferometric wavelength converters were reported [26–34]. Further, optical gates based on Mach–Zehnder interferometric (MZI) and SOA as the nonlinear element have attracted much interest due to practical advantages [35–40]. SOA–MZI has extremely high operational speed, tremendous potential for integration with a wide variety of active and passive components, low power consumption, and high stability. Various all-optical logic-based SOA–MZI switches with XOR, OR, NOR, and NAND functions were reported, and so also were half-adder and full-adder units [35–40].

Therefore, to match the operational speed of digital optical systems and optical processors, ultra-fast and all-optical logical elements are needed to perform arithmetic operations. In this regard, in this paper, we combine the attractive and powerful parallelism property of the MSD number representation with the ultra-fast all-optical switching property of the SOA–MZI switch to design and implement all-optical MSD arithmetic circuits. The proposed MSD adder/subtracter optical circuits are fully parallel schemes and the operational speed of the optical switches is extremely high (far above gigahertz). Consequently, the proposed adder circuits will be very helpful in developing hardware modules for optical digital computing processors. Several all-optical circuit designs are proposed in order to minimize the number of the SOA–MZI switches as well as the time delay in the adders. Two bits per digit binary encoding of the trinary MSD digits are employed in order to use the switching property of the SOA–MZI unit.

2. Modified signed-digit number

A decimal number D can be represented by an n-digits MSD number as $D = \sum_{j=0}^{n-1} X_i 2^j$ where X_i is a member of the set $\{\bar{1}, 0, 1\}$. Here $\bar{1}$ denotes -1. An MSD negative number is the MSD complement of the MSD positive number. For example, using primes to denote complementation, we have $\bar{1}' = 1$, $1' = \bar{1}$, $0' = 0$, and therefore $(-3)_{10} = [0\ \bar{1}\ \bar{1}]_{\mathrm{MSD}}$ or, equivalently $(-3)_{10} = [\bar{1}\ 0\ 1]_{\mathrm{MSD}}$. The addition of two MSD numbers involves three steps (see Table 1 and Fig. 1): the first two steps will generate transfer (T_i) and weight (W_i) digits. The third step will produce the result. The T_i and W_i digits are generated in parallel as the operands flow through the processing architecture, making addition of any length operands occur in the same amount of time. In Fig. 1, the A, B, and C blocks represent the three-step addition rules of Table 1. For subtraction, the complement rule is applied first and then an addition is performed.

By incorporating additional information from the next less-significant pair of digits $x_{i-1}y_{i-1}$ (see Table 2 and Fig. 2), a simpler addition is obtained [17]. In Fig. 2, the A and B blocks represent the addition rules of

Table 1. Addition rules for the classical three-step MSD adder scheme.

step 1

$x_i y_i$	$1\,1$	$\begin{matrix}0\,1\\1\,0\end{matrix}$	$0\,0$	$\begin{matrix}1\,\bar{1}\\\bar{1}\,1\end{matrix}$	$\begin{matrix}0\,\bar{1}\\\bar{1}\,0\end{matrix}$	$\bar{1}\,\bar{1}$
T_{i+1} / W_i	1 / 0	1 / $\bar{1}$	0 / 0	0 / 0	$\bar{1}$ / 1	$\bar{1}$ / 0

step 2

$T_i\ W_i$	$1\,1$	$\begin{matrix}0\,1\\1\,0\end{matrix}$	$0\,0$	$\begin{matrix}1\,\bar{1}\\\bar{1}\,1\end{matrix}$	$\begin{matrix}0\,\bar{1}\\\bar{1}\,0\end{matrix}$	$\bar{1}\,\bar{1}$
T_{i+1} / W_i'	1 / 0	0 / 1	0 / 0	0 / 0	0 / $\bar{1}$	$\bar{1}$ / 0

step 3

$T_i' W_i'$		$\begin{matrix}0\,1\\1\,0\end{matrix}$	$0\,0$	$\begin{matrix}1\,\bar{1}\\\bar{1}\,1\end{matrix}$	$\begin{matrix}0\,\bar{1}\\\bar{1}\,0\end{matrix}$	
S_i / $\bar{S}_i$		1 / $\bar{1}$	0 / 0	0 / 0	$\bar{1}$ / 1	

Complement

$x_i y_i$	$1\,1$	$\begin{matrix}0\,1\\1\,0\end{matrix}$	$0\,0$	$\begin{matrix}1\,\bar{1}\\\bar{1}\,1\end{matrix}$	$\begin{matrix}0\,\bar{1}\\\bar{1}\,0\end{matrix}$	$\bar{1}\,\bar{1}$
$x_i \bar{y}_i$	$1\,\bar{1}$	$\begin{matrix}0\,\bar{1}\\1\,0\end{matrix}$	$0\,0$	$\begin{matrix}1\,1\\\bar{1}\,\bar{1}\end{matrix}$	$\begin{matrix}0\,1\\\bar{1}\,0\end{matrix}$	$\bar{1}\,1$