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Congestion-Driven Multilevel Full-Chip Routing Framework*

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Abstract: A W-shaped multilevel full-chip routing framework using W-shaped optimization flow is used to find the final routing solution. The W-shaped flow consists of two sequential V-shaped optimization flows. The first V-shaped flow optimizes the global routing solution. The probabilistic congestion prediction technique is used to guide the global routing decision to find the routing solution that evenly distributes the nets. Then, the second V-shaped flow improves the quality of the routing result. Tests on a set of commonly used benchmark circuits and comparisons with other multilevel routing systems show that the routability, total wire length, total number of vias, and the runtime are all improved.

Key words: physical design; multilevel routing; full-chip routing; congestion

Introduction

As circuit designs shrink, very large scale integrated circuites (VLSI) designs are becoming more and more complex[1]. The highly complex routing problems are often solved using a divide-and-conquer approach. Traditional methods have used two sequential stages of global routing followed by a detailed routing analysis to find the final routing solution. During the global routing stage, the routing area is dissected into rectangular routing tiles with the global router determining wirings for each net across the tiles. After the global routing, the detailed router decides the exact connections for nets inside the individual tiles for each tile. The literature describes many global and detailed routing algorithms for the two-stage routing frameworks.

As VLSI technology advances into nanometer sizes, the traditional two-stage routing framework is confronted with two major challenges of the ever increasing design complexity of gigascale integration and the concomitant complicated physical effects. The continuously increasing routing problem size has given birth to a new routing methodology using multilevel routing[2] which has proven to be much more effective for large routing problems. The framework features a V-shaped flow of an iterative coarsening stage followed by an iterative uncoarsening refinement stage. Cong et al.[3] made improvements to make the framework more effective (This framework is implemented as MARS). Cong and Zhang[4] adopted the framework for thermal-driven 3-D routing. The multilevel routing framework has significantly improved routing designs; however, some deficiencies still exists.

(1) During the coarsening stage, the resource reservation technique, which confines the short nets to small numbers of patterns to reduce the routing resources, is quite primitive. The constraint on the patterns of short nets may affect the solution space and, thus, lose good solutions for the entire routing problem. The probabilistic congestion estimation method gives more reasonable results for the coarsening stage with much less restrictions on the net patterns.

(2) The MARS framework performs only global routing solutions, so the results must be fed to a detailed router for the final routing solution. Since the differences between global routing and detailed routing

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tend to hide the detailed routing information from the global router, improper global routing decisions often occur. Detailed routing algorithms shall be integrated into the framework to bridge the gap. This integration can provide valuable accurate routing resources and congestion information for the subsequent global routing process.

Lin and Chang[5] proposed another multilevel routing (MR) framework for grid-based routing. Unlike Cong et al.[2], MR integrates global routing, detailed routing, and resource estimation during the two routing stages of the V-shaped flow. On the downward pass, the global routing is based on pattern routing, while on the upward pass, the pattern router is changed to a maze router to refine the nets that failed on the downward pass. MR has successfully solved the routing problem with high routing completion rates and short runtimes. Improvements have been made to adapt the framework to consider performance, antenna effects, and X-based architectures[6-8]. Chen and Chang[9] provided a gridless routing framework, using optical proximity correction (OPC). As with MARS, some improvements are also possible for the MR framework.

(1) Before routing, the nets are decomposed into two-term subnets using the minimum spanning tree algorithm, which generally results in longer wire lengths than Steiner tree-based net decomposition.

(2) During the coarsening stage, the nets are routed one by one using an enumeration pattern global router followed by a maze detailed router. The sequential net routing order decided by the coarsening process is not systematic.

(3) Although the enumeration global routing method improves the routing completion rate, it lacks a global routing strategy and, thus, can easily create local congestion in congested designs.

Therefore, this paper prevents a grid-based W-shaped multilevel routing (WMR) framework which has the following distinguishing features:

(1) The framework consists of two coarsening stages and two refining stages which form two "V" shapes, i.e., the "W" shape. The first V-shaped flow (V_1) seeks global routing results for all the nets with good congestion distribution. Then, the second V-shaped flow (V_2) integrates the global routing and the detailed routing together to find the final routing solution with an optimized wire routing layout and improved completion rate.

(2) A probabilistic congestion prediction before the W-shaped optimization flow generates congestion information is used to guide the global routing decision during the V_1 routing stage.

(3) During the first coarsening stage, the net redistribution heuristic is used to redistribute short nets from higher levels down to lower levels. The net redistribution technique makes the net ordering more natural and reasonable.

(4) Multi-pin nets are decomposed into two-pin subnets using the FLUTE Steiner tree heuristic[10] instead of the minimum spanning tree algorithm. The Steiner pin relocation heuristic is used to improve the routing completion rate.

1 Overview of WMR Framework

The WMR routing flow shown in Fig. 1 can be partitioned into five stages. The first stage is the pre-routing stage during which all the multi-pin nets

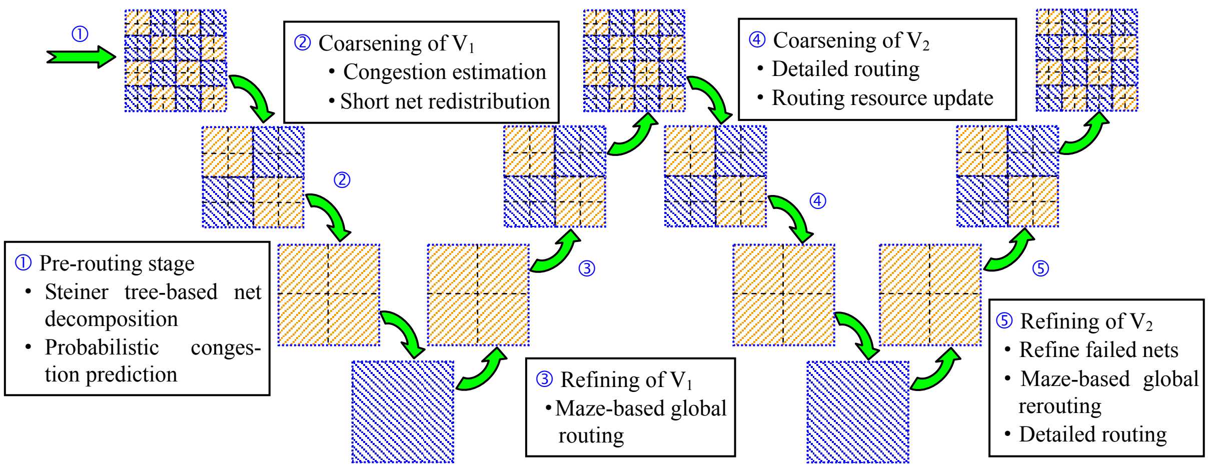

Fig. 1 WMR routing flow