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An application of reconfigurable technologies for non-invasive fetal heart rate extraction

D.P. Morales*, A. García, E. Castillo, M.A. Carvajal, L. Parrilla, A.J. Palma

ECsens, Department of Electronics and Computer Technology, ETSIIT, University of Granada, Granada, Spain

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This paper illustrates the use of a reconfigurable system for fetal electrocardiogram (FECG) estimation from mother's abdomen ECG measurements. The system is based on two different reconfigurable devices. Initially, a field-programmable analog array (FPAA) device implements the analog reconfigurable preprocessing for ECG signal acquisition. The signal processing chain continues onto a field-programmable gate array (FPGA) device, which contains all the communication and interfacing protocols along with specific digital signal processing blocks required for fundamental period extraction from FECG waveforms. The synergy between these devices provides the system the ability to change any necessary parameter during the acquisition process for enhancing the result. The use of a FPGA allows implementing different algorithms for FECG signal extraction, such as adaptive signal filtering. Preliminary works employ commercially available development platforms for test experiments, which suffice for the processing of real FECG signals from biomedical databases, as the presented results illustrate.

1. Introduction

Early information about fetus status during gestation and labor is the principal tool for detecting possible damages in the fetus physiological conditions. One of the main sources of information is the fetal heart rate (FHR) measurement through different techniques that comprise cardiotocography (CTG) and electrocardiogram (ECG) [1]. Noninvasive electrical activity detection techniques offer a method for estimating this status by obtaining magnitudes such as fetal electrocardiogram (FECG) and fetal electroencephalogram [2]. In particular, noninvasive FECGs are measured along with maternal electrocardiogram (MECG) using skin electrodes over the mother's abdomen. The FECG is separated from the maternal signal using digital processing techniques, which are computationally demanding [3,4] and are continuously improved [5,6], since FECG is an extremely low-voltage signal compared to maternal ECG.

This paper presents a FECG acquisition and processing system based on reconfigurable analog and digital devices that work in conjunction. By means of this device arrangement, FECG and MECG signals are acquired and analogically conditioned by the field-programmable analog array (FPAA) device. While a variety of alternatives are commercially available for analog conditioning, FPAAs offer the possibility of total reconfigurability with a wide range of implementable blocks, just in the same way that field-programmable gate arrays (FPGAs) allow digital reconfiguration. Thus, a fixed architecture can be reconfigured for accommodating very different analog conditioning structures. FPAA's differential input ports offer a low-noise, low-offset amplifier that suits the intrinsically differential ECG signals. Internal reconfigurable processing blocks allow filtering and posterior amplification. Subsequently, these signals are digitalized and processed in a FPGA device. In this application, which shows the processing advantages inherent to the association of these devices, signal separation is performed through an adaptive filtering technique and the FHR is obtained. As for the analog subsystem, other choices are possible, with microprocessors, microcontrollers and digital signal processors being the most popular. However, FPGA offers more profound and more hardware related reconfiguration options, also allowing for increased data throughput as custom processing blocks may be implemented, while also embedded processing are also possible. Thus, the use of a FPGA device provides the possibility for implementing other processing circuits, such as FIR or wavelet filtering among others [7], without the need of hardware redesign. This compounded reconfigurable system shows versatility that outperforms other possible solutions, such as programmable-system-on-chip (PSoC) [8], since the amount of resources is wider in both reconfigurable fields, allowing implementing more elaborated processing structures. The overall system has been previously tested, showing its capacity for accommodating applications very different in

* Corresponding author at: Dpto. Electrónica y Tecnología de Computadores. Universidad de Granada, ETSIIT, Periodista Daniel Saucedo Aranda, 18071 Granada, Spain. Tel.: +34 95824 8845.
E-mail address: diegopm@ugr.es (D.P. Morales).

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nature. In previous works [9–11], this system has been employed for environmental temperature and pressure measurement. This structure allowed incorporating commercial sensors to the IEEE-1451 compliant standard for smart sensors. Additionally, using reconfiguration techniques, the system was used for increasing the resolution of the analog-to-digital converter configured in the FPAA. In a completely different orientation, the same system has been also used for ECG signal conditioning, providing reliable results [12] while showing the benefits of the use of reconfigurable technologies. Thus, the same hardware platform previously used for a number of applications quite far from biosignal processing [9], can be applied to ECG acquisition and processing with no hardware change, just reconfiguration, so this work will be extended here by expanding this scenario to the more complex problem of FECG acquisition, processing and FHR extraction. While the use of ASICs (Application Specific Integrated Circuit) is a costly solution for ECG conditioning and feature extraction that requires considerable design time and cost [13,14], the proposed system provides an economical and fast-prototyping platform, which could be even used in short and medium scale production. This work thus extends the previous ECG application and opens the use of this system to fetal ECG acquisition and heart rate extraction. This new task requires a completely new implementation, with a second analog path in the FPAA and a different digital processing hardware in the FPGA. However, due to the nature of the processed signals which are acquired in the same fashion that ECG signals, the results presented in the previous work [12] are a precedent that supports this work.

The work is structured as follows: Section 2 presents the particular features of noninvasive FECG acquisition and the analog and digital processing required for this kind of signals. Section 3 presents the system architecture, which is the base for the application developed and consists mainly of a FPAA and a FPGA. Section 4 outlines the performance of the analog processing implemented in the FPAA using synthetic FECG plus MECG signals. Additionally, the digital processing algorithm for FECG extraction implemented in the FPGA device is tested. For this aim, real ECG signals of pregnant women from public biomedical databases are used. Section 5 depicts the complete system, and the results for real-time acquisition and extraction experiments are presented. Section 6 discusses, having in mind the results in the previous section, the main advantages of this platform when compared other approaches in the literature. Finally, the main conclusions of this work are summarized in Section 7.

2. Fetal electrocardiogram features

Fetal noninvasive electrocardiogram signals, acquired over the mother's abdomen, are weak signals, with maximum amplitudes around 600 μV, that are mixed with other biological electrical signals, such as myographic signals, movement electrical artifacts and encephalograph signals from both mother and fetus, apart from external interference sources such as power line interference, i.e., electromagnetic radiation absorbed by wire connections and electrodes, and the thermal noise generated within the acquisition electronics. But over all other noise sources, the FECG is compounded with the mother ECG, which has amplitudes that exceed FECG amplitude by an order of magnitude. This signal weakness and noisy environment do not allow using noninvasive FECG for detecting structural defects on fetal heart, due to hardware limitations for the acquisition and processing of a truly fetal ECG shape that would allow diagnosis of fetal heart diseases [7]. On the other hand, it is feasible to extract from these signals the fetus heart rate, which has been shown to be a reliable instrument for diagnosis of fetal ischemia related to umbilical cord strangulation. Other techniques, such as Doppler ultrasound monitoring of the fetal heart rate, introduce energy from the bulky transducer to the fetus. This circumstance limits the use of these techniques in long-term monitoring tasks. Due to its inherent noninvasive nature, abdominal FECG recordings are convenient for fetal heart rate extraction [15].

2.1. Attributes of FECG signal analog acquisition

A typical FECG analog acquisition system consists of an analog stage that collects the signal with various electrodes attached to the mother skin. Usually, when an 8-electrode ECG acquisition system is employed, three electrodes are attached to maternal thorax and five are distributed over the maternal abdomen [16]. The thorax electrodes provide the mother ECG without the fetal component and the abdominal electrodes provide the compounded signal.

Given the weak amplitude of the FECG signal, which is immersed in the mother one, the analog system is required to amplify the signal and reduce the environment-induced noise to allow a further digital extraction of the fetal heart rate. Usual analog conditioning for each electrode channel, as shown in Fig. 1, includes an initial amplification stage prior to the filtering stages that comprise a high-pass filter followed by a notch filter, and finally a low-pass filter. This filter arrangement allows to select the range of frequency components in an ECG, which ranges from 0.01 to 150 Hz, although recent works suggest that this range must be extended to 500 Hz [7]. The notch filter central frequency is set to the characteristic 50/60 Hz of the power line. Other elements to keep in mind are the analog-to-digital converter (ADC) resolution and sampling frequency. If a low resolution ADC is used, the analog chain must use low noise and high gain (approximately 1000) voltage amplifiers. On the other hand, with high resolution ADCs the amplifiers are allowed to have lower gains.

Typical ECG analog front-end systems are designed using discrete off-the-shelf devices [17] that implement each of the modules in Fig. 1. However, applications such as low-voltage, portable (or lately wearable) ECG systems may require custom PCB (Printed Circuit Board) [18] or even ASIC [19] designs. This paper offers a different option based on an analog reconfigurable device that implement the analog ECG front-end, which allow redesigning the elements within the conditioning chain, along with a digital configurable device that can host the required digital signal processing and be reconfigured as required. These reconfigurability capabilities may be used in FECG acquisition, thus allowing selecting the amplification gain and/or filtering corner frequencies for each channel, which facilitates the subsequent digital fetal heart rate extraction. An implementation on a PCB with components off-the-shelf offers a rigid structure that may be cheaper for a specific application but that does not allow facing any different applications, which could range from environmental parameter measurement and sensor standardization under the IEEE 1451 [9], to ADC resolution enhancing through analog reconfigurations [10].

2.2. Fetal heart rate extraction

Once the compounded (mother and fetus) ECG signals from each electrode are conditioned and digitalized, the subsequent stage must perform the fetal heart rate extraction. There are different signal processing techniques that have been proposed for fetal R-wave detection, such as nonlinear and linear decomposition methods that include wavelet decomposition and independent component analysis (ICA), among others [7]. ICA methods outperform most of the other techniques, but are computationally demanding and are not directly appropriate for real-time applications [5]. On the other hand, adaptive filtering, i.e., adaptive noise cancellation, is a less demanding processing technique that has been widely implemented for maternal ECG cancellation and FECG extraction [3]. The procedure uses thoracic leads as reference signals to eliminate the