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Efficient methods of initializing neuron weights in self-organizing networks implemented in hardware

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ABSTRACT

In this paper, we focus on the topic of an efficient initialization of neuron weights, which is one of key problems in artificial neural networks (ANNs). This problem is important in ANNs implemented as Application Specific Integrated Circuits (ASICs), in which the number of the weights is relatively large. When ANNs are implemented in software, the weights can be easily modified. In contrast, in neural networks realized as ASICs in which due to parallel data processing each neuron is realized as a separate circuit, it is necessary to provide programming and addressing lines to each memory cell containing a weight. This causes a substantial increase in the complexity of such systems. In this study, we performed comprehensive investigations, in which we simulated the training process of the Self-Organizing ANN with different initialization scenarios. The aim of these investigations was to find simple and efficient initialization procedures that lead to optimal learning process for a broad spectrum of values of other network parameters.

The investigations have shown that Self-Organizing Maps (SOMs) in many situations may be trained without any initialization (with zeroed weights). This is possible due to the neighborhood mechanism that to some degree stimulates the neurons belonging to the SOM. We present selected results of several thousands simulations for different topologies of the SOM, for different neighborhood functions and two distance measures between the learning patterns and neurons in the input data space. Simulations were performed for initial values of the weights equal to zero, for small values (up to 1% of full scale range) and for neurons randomly distributed over the overall input data space. The results in most cases are comparable that allows to reduce the complexity of the SOM implemented in the CMOS technology.

1. Introduction

Artificial neural networks (ANNs) are used in many fields of engineering, especially in data mining and classification. They allow to detect abnormal situations in large datasets, which is useful in image processing, medical diagnostics, but also to

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some extent cope with in control engineering problems [1,2]. Designing neural networks (NNs) can be considered from two points of view. Typically the investigations rely on developing new training algorithms or modifying existing ones in order to obtain better learning quality in specific real situations. On the other hand, there exists another class of problems that relies on an efficient hardware implementation. In the literature one can find various types of such realizations of NNs that include Field Programmable Gate Arrays (FPGAs) [3–5] and Very Large Scale of Integration (VLSI) ASICs with full custom approach [6–8]. The second approach requires solving specific, usually challenging, problems related to circuit structure or in many cases even of physical nature. Such design process is time consuming, however ANNs implemented in this way offer strong abilities of parallel data processing at very low power dissipation. These features make them much more efficient than their FPGA counterparts [9,10], and simultaneously much faster than in case of software realizations. The power dissipation can be even four orders of magnitude lower than in PC realizations [8,9,11]. These features make ASIC realizations suitable for the application in new areas, for example, in Wireless Body Sensor Networks (WBSNs) used in medical diagnostics [12].

The presented work is one of the important steps in a project that aims at development of a new chip based on ANNs, suitable for WBANs. Such systems usually consist of a set of tiny devices (sensors), each equipped with a biosensor or a set of biosensors, allocated or implanted in the human body close to the place of data acquisition. Such devices communicate wirelessly with a base station providing collected data for a further processing and mining. In contrary to typical WBAN sensors that perform only basic tasks that rely on data collection and transmission, the proposed solution will allow for data processing and classification directly in the sensors. This is an important advantage. One of the main problems encountered in such systems today is very large energy lost (even 90%) during the radio-frequency (RF) wireless transmission. This strongly reduces the battery lifespan [13] and thus is one of the barriers in a development of truly wearable medical systems, convenient for the patients. We propose novel, intelligent and more autonomous sensors, equipped with low power ANN, that will be able to preform data analysis and classification on board, and thus will reduce the amount of data transmitted to the base station.

In our investigations, we focus mostly on self-organizing learning algorithms, as they offer relatively simple structures with usually only simple arithmetic operations such as additions, subtractions, multiplications, shifting the bits and the abs() function. Nevertheless, such ANNs has been shown to be suitable for the analysis of various biomedical signals, including ECG signals [2,14].

In this study, we focus on the problem of efficient initialization of neuron weights and influence of this process on the learning quality of Self-Organizing Maps (SOMs). Our interest in this problem results from the fact, that initial values of the weights exhibit a great influence on the hardware complexity of the system. We demonstrate that in many cases the initialization phase can be omitted, as the neighborhood mechanism is able to activate all neurons in the SOM. To provide reliable results we performed comprehensive investigations for different sizes of the map and different configurations of other parameters. The aim of these investigations was to reduce the chip area of the system that will reduce the fabrication costs, as well as the power dissipation. Preliminary results on this topic were presented by us in [15]. This study significantly expands the scope of the research presented there. We also present here several possible ways of hardware implementation, not presented so far.

The presented work is one of the steps in a bigger project that aims at a full implementation of a programmable SOM in the CMOS technology, for the application in portable devices. The system itself will be very complex and thus requires comprehensive investigations in every aspect. Each mechanism and component of the SOM had to be invented from scratch and optimized in terms of an efficient transistor level implementation. The presented work is devoted to the initialization and programmability problem, however, it has to be presented in a wider perspective. For this reason we recall some details concerning the project as a whole. For example, the evaluation process of the SOM is based on five assessment criteria. Optimization of each component of the SOM was performed by us on the basis of a similar scheme, i.e. through comprehensive simulations of the learning process for different values of selected parameters. During such process we always use these assessment criteria and therefore we also present them in this paper, for a better clarity. In our former works we focused in detail on the neighborhood mechanism [9], the neighborhood function [11], the distance calculation circuit [16], the conscience mechanism [8], the adaptation mechanism [17]. The main objective off all these investigations was to strongly reduce the number of transistors to safe the silicon area and to reduce the power dissipation. The purpose of the investigations presented in this work is very similar. Our objective is to check if and how the initialization mechanism can be optimized to reduce the computational and hardware complexity.

The paper is organized as follows. In next section we briefly present the Kohonen SOM optimized for an efficient parallel hardware realization, as well as methods suitable for quantitative investigations of the learning process. In this Section we also make an overview of existing initialization methods, which is a background for the investigation results and their assessment presented in following two Sections. Sections 3 and 4 are devoted to a quantitative comparison and discussion of the obtained results. In these Sections we present detailed simulations performed by means of the software model of the SOM. The purpose of these investigations was to determine the influence of the initial values of the neuron weights on the quality of the learning process. Section 5 presents several possible ways of hardware implementation of the initialization mechanism. Finally, we formulate the conclusions.

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