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Efficient design of silicon slot waveguide optical modulator

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ABSTRACT

An optimal design of a slot waveguide is presented for realizing an ultrafast optical modulator based on a 220 nm silicon wafer technology. The recipe is to maximize the confinement and interaction between optical power supported by the waveguide and electric field applied through metallic electrodes. As height of waveguide is fixed at 220 nm, the waveguide and slot width are optimized to maximize the confinement factor of optical power. Moreover, metal electrodes tend to make the waveguide lossy, their optimal placement is calculated to reduce the optical loss and enhance the voltage per unit width in the slot. Performance of an optimally designed slot waveguide with metal electrodes as ultrafast modulator is also discussed.

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1. Introduction

Silicon photonics offer a powerful platform for photonic integrated circuits (PIC's). Nowadays, silicon is one of the promising materials to provide high integration at low cost using a well established silicon-on-insulator (SOI) based CMOS (Complementary Metal Oxide Semiconductor) fabrication technology [1–3]. However, silicon has a centro-symmetrical crystal structure. Therefore, silicon does not show second order nonlinearity (χ^2). SOI technologies overcome the problem and provide integration of a linear electro-optic (EO) polymer with silicon. This platform combines the electronics and optical effect to fulfill the requirement of ultrafast photonic devices [4].

The low index EO polymer is well suited for a slot optical waveguide which is a current topic of great interest for researchers [5]. Slot optical waveguide is fabricated through high index waveguides separated by a low index material slot of few nanometers (nm). Due to a large discontinuity of electric field at low and high refractive indices' boundary, optical electric field is confined in a low index region slot and confinement is manifold times greater than that in conventional waveguides like rib, buried and channel waveguides [5]. The interaction of applied electric field to propagating electromagnetic wave in a slot filled EO polymer is proposed for low dimension PIC devices like modulators [6,7], switches [8], sensors [9], splitters [10] and couplers [11]. Another aspect of a slot waveguide is to fulfill all time requirements of optical communication such as small dimension in comparison to another waveguide, low voltage- length product, high modulation efficiency, low power consumption, and high data rate support. Minimized half-wave voltage-length (V_π-L) product can be achieved through: a) high EO coefficient and, b) maximum overlap of static electric field with optical field in EO material [12]. The narrow separation of an electrode from waveguide edges leads to a significant loss which increases optical absorption and propagation loss per unit length in a modulator [12,13]. Therefore, optimal separation of electrodes is essential to reduce losses of propagating modes.

In this paper, a design procedure of electro-optic modulator based on a 220 nm silicon wafer technology with a polymer filled slot optical waveguide is proposed which can be converted easily into layouts that can be transferred on to PIC. First, optical waveguide is optimized for high confinement of electric field in a polymer filled low index slot. Next, optimization of the electrode distance from the silicon waveguide is considered for the lowest possible optical absorption and maximum interaction of an optical field with applied voltage.

2. Design consideration for a slot waveguide

The schematic diagram of vertical slot waveguide electro-optic modulator is shown in Fig. 1. It consists of a low index vertical narrow slot sandwiched between two high index rectangular waveguides. The high index rectangular waveguide is formed with a 220 nm silicon (refractive index $n_f = 3.48$) on standard SOI wafers with a 2 μm silicon oxide (SiO_2) (refractive index $n_{sub} = 1.46$) [5]. Low index electro-optic polymer is filled in slot region which has the electro-optic coefficient (r_{33}) 100 pm/V and the refractive index (n_s) 1.7. In this simulation, it is assumed that electrodes of silver ($n_{silver} = 0.4096 + j10.048$) and separated from silicon waveguide by

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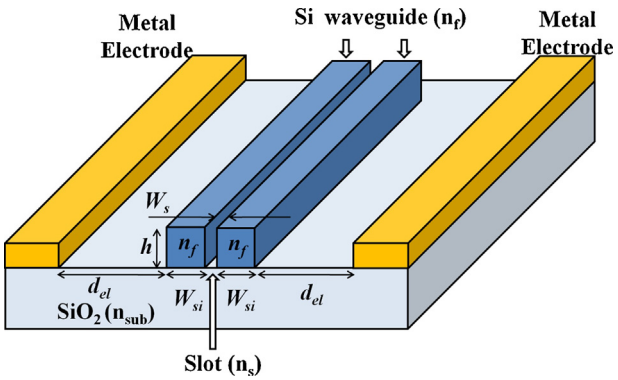

Fig. 1. Schematic diagram of a slot optical waveguide modulator.

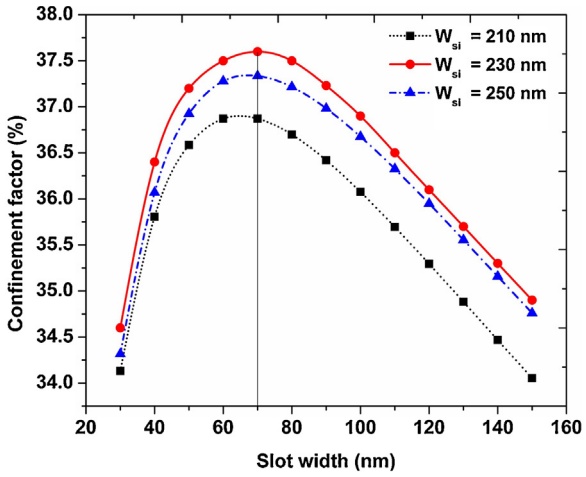

Fig. 2. Variation of a confinement factor in slot waveguide as a function of slot width for different silicon waveguide widths of 210 nm, 230 nm, and 250 nm.

the distance d_{el} which has to be optimized. In this paper, all simulations are performed for a low loss communication window of 1550 nm. The waveguide geometry is optimized for high confinement of electric field in slot based on confinement factor (Γ) which can be defined as ratio of power confined in slot region to total power in guiding region as given below [14,15]:

$$\Gamma = \frac{\iint_{slot} |E_x|^2 dxdy}{\iint_{total} |E_x|^2 dxdy} \quad (1)$$

For the parametric analysis of a silicon slot waveguide, the finite element method (FEM) based commercial solver COMSOL is utilized.

2.1. Optical confinement

The optical confinement for efficient electro-optic modulators are investigated for different slot waveguide dimensions to realize an optimal modulator. The modulator geometry is optimized on the basis of confinement of electric field intensity in slot region through intensity confinement factor of quasi-TE mode.

The several combinations are considered for the slot waveguide width (W_s) and the silicon waveguide width (W_{si}) with the constant height (h) of 220 nm, limited by the silicon wafer technology. The iterative parametric simulation results are shown in Fig. 2 with variation in a slot width from 30 nm to 150 nm for different silicon

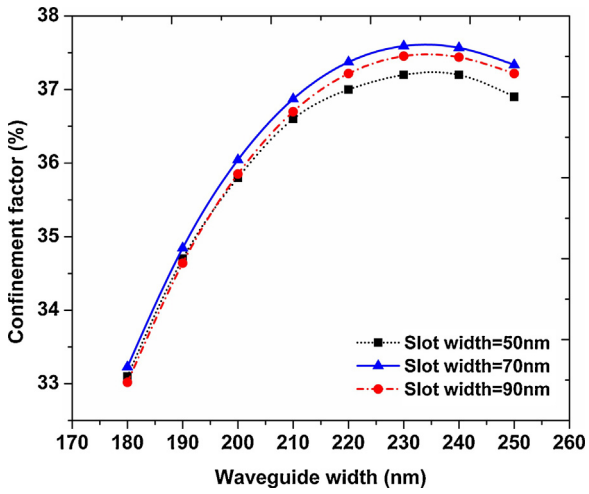

Fig. 3. Variation of a confinement factor in slot waveguide as a function of silicon waveguide width for different slot widths of 50 nm, 70 nm, and 90 nm.

waveguide widths of 210 nm, 230 nm, and 250 nm. Fig. 2 illustrates that for physical parameters selected in the present study, confinement factor peaks at a slot width of 70 nm for all waveguide widths. However, for the waveguide width of 230 nm maximum the value of confinement factor is of 37.59% which is 5% more than the 32.6% for a reported wider slot of 200 nm [7]. Further, confinement factor is obtained for different slot widths of 50 nm, 70 nm and 90 nm as a function of silicon waveguide width varying from 180 nm to 250 nm and is shown in Fig. 3.

It can be seen from Fig. 3 that the confinement factor increases with silicon width and peaks at 230 nm for all slot widths (W_s) with maximum value for a 70 nm slot width (37.59%). The optimized slot geometry with optical mode in slot is shown in Fig. 4. The surface plot of the electric field distribution (E_x) is shown in Fig. 4(a) that shows optical electric field confined in a narrow low index slot waveguide is high as compared to adjacent silicon waveguides. The corresponding electric field distribution in x direction at y = 1110 nm is shown in Fig. 4(b) which shows discontinuity at the boundaries. Similarly, electric field distribution in y direction at x = 0 is shown in Fig. 4(c).

Even if the slot waveguide is optimized for a high confinement of electromagnetic field in slot, there is possible loss in a guided optical mode when metal electrodes are put adjacent to high index silicon waveguides. Therefore, placement of electrodes with respect to the silicon waveguide is vital important since they contribute mode loss due to absorption of optical field in the metal [13]. This absorption loss leads to a propagation loss along the length. The complex modal index of fundamental quasi TE eigenmode distribution of slot waveguide is calculated as $n = n_{eff} + jn_{ieff}$ where n_{eff} and n_{ieff} are effective index and extinction coefficient, respectively. The absorption loss of optical mode in metal electrode is determined through imaginary effective index known as extinction coefficient. The absorption loss (α) is expressed as [13]:

$$\alpha \frac{40\pi n_{ieff} \log e}{\lambda} \quad (2)$$

where e is the natural constant. For silicon waveguide widths (W_{si}) of 210 nm, 230 nm and 250 nm and fixed slot width (W_s) of 70 nm absorption loss is obtained, as a function of electrode distance (d_{el}) from silicon waveguide outer edge and are shown in Fig. 5. From the simulation results, strong imaginary part of modal index is found which is responsible for absorption losses in optical mode. In this simulation, it is assumed that silicon is lossless at communication wavelength and waveguide surface roughness is also ignored. It can also be observed from Fig. 5 that if electrodes are placed at

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