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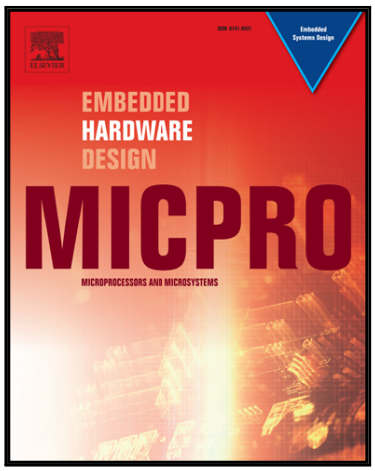

HAPE: A High-level Area-Power Estimation Framework for FPGA-based Accelerators

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PII: S0141-9331(17)30563-X
DOI: https://doi.org/10.1016/j.micpro.2018.08.004
Reference: MICPRO 2731

To appear in: *Microprocessors and Microsystems*

Received date: 15 December 2017
Revised date: 26 July 2018
Accepted date: 9 August 2018

Please cite this article as: Mariem Makni, Smail Niar, Mouna Baklouti, Mohamed Abid, HAPE: A High-level Area-Power Estimation Framework for FPGA-based Accelerators, *Microprocessors and Microsystems* (2018), doi: https://doi.org/10.1016/j.micpro.2018.08.004

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HAPE: A High-level Area-Power Estimation Framework for FPGA-based Accelerators

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Abstract

Recent embedded applications are widely used in several industrial domains such as automotive and multimedia systems. These applications are critical and complex, involving more computing resources and therefore increasing the power consumption of the system. Although performance still remains an important design metric, power consumption has become a critical factor for several systems, particularly after the increasing complexity of recent System-on-Chip (SoC) designs. Consequently, the whole computing domain is being forced to switch from a focus on high performance computation to energy-efficient computation. In addition to the time-to-market challenge, designers need to estimate, rapidly and accurately, both area occupation and power consumption of complex and diverse applications. High-Level Synthesis (HLS) has been emerged as an attractive solution for designers to address this challenge in order to explore a large number of design points at a high-level of abstraction. In this paper, we target FPGA-based accelerators. We propose HAPE, a high-level framework based on analytic models for area and power estimation without requiring register-transfer level (RTL) implementations. This technique allows to estimate the required FPGA resources and the power consumption at the source code level. The proposed models also enable a fast design space exploration (DSE) with different trade-offs through HLS optimization pragmas, including loop unrolling, pipelining, array partitioning, etc. The accuracy of our proposed models is evaluated by using a variety of synthetic benchmarks. Estimated power results are compared to real board measurements. The area and power estimation results are less than 5% of error compared to RTL implementations.

Keywords: HLS; SoC; Hardware accelerator; RTL; FPGA; DSE

1. Introduction

Embedded System-on-Chips (SoCs) have often conflicting constraints such as time and energy which considerably harden the design of those systems. In addition, complex embedded applications have to cope with an increasing demand of functionalities, which require increasing processing capabilities [1][2].

With the introduction of heterogeneous computing systems such as the Xilinx Zynq UltraScale+ multiprocessor system-on-chip (MPSoC) [3], different processing units can be embedded in the SoC to meet the growing requirements of the applications (performance/power constraints). Complex applications include different computing-intensive functions with multiple nested loops. This leads to significantly increased power consumption as well as higher processing requirements to ensure the respect of constraints expected in such systems. Consequently, designers need to estimate the various design metrics (execution time, area, power) of the embedded system at the earliest step in the design flow.

High-Level Synthesis (HLS) [4][5] tools have been developed in the recent years to address this challenge. These tools are used to automatically generate circuit specifications in hardware description language from high-level languages (e.g., C/C++) without the need for time-consuming manual register-transfer level (RTL) generation [6]. The utilization of these tools significantly saves time and programming effort.

In addition, HLS tools provide various optimization pragmas such as loop unrolling, pipelining, array partitioning, etc. [7][8]. This enables designer to explore the large number of potential design points for an application with these pragmas while optimizing for performance and/or area constraints. Unfortunately, the large design space resulting from the different pragma combinations makes exhaustive design space exploration (DSE) a time-consuming task. Consequently, the runtime of the HLS tools is prohibitively long to exclude the possibility of exhaustive design space, especially for complex designs.

Analytic models have been proposed to address these challenges by enabling a rapid design space exploration

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