An efficient and low power one-lambda crosstalk avoidance code design for network on chips

Zahra Shirmohammadi[a,*], Zeinab Mahdavi[b]

[a] *Shahid Rajaee Teacher Training University, Tehran, Iran*
[b] *Department of Computer Engineering, Sharif University of Technology, Tehran, Iran*

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ABSTRACT

Crosstalk faults occurring in wires of Networks on Chip (NoCs) can seriously threaten the reliability of data transfer. One efficient way to tackle crosstalk faults is numeral-based Crosstalk Avoidance Codes (CACs). Numeral-based CACs reduce crosstalk faults by preventing specific transition patterns to occur. One-Lambda Codes (OLCs) are the most efficient types of CACs. However, the codec of OLCs imposes overheads including power consumption, critical path and area occupation to the routers of NoCs. To find overhead-efficient OLCs, this paper proposes an Algorithm for Generating OLC Numeral systems (AGON). AGON provides a tradeoff for designers in selecting overhead-efficient OLCs. Using AGON, an efficient numeral-based OLC called Subtraction-based-Numeral (Sub-Num) is proposed that benefits the Numeral system that can omit OLC-induced transition patterns completely. In addition, the mapping algorithm of Sub-Num can reduce the overheads of codec more efficiently than the other state-of-the art OLCs. Evaluation results using SPICE and VHDL simulations show that Sub-Num reduces power consumption and average delay of wires by 10% and 9%, and also overheads of codecs including dynamic power consumption, critical path and area occupation by 52%, 51% and 21%, respectively as compared to the state-of-the-art numeral-based OLC.

1. Introduction

Network on Chip (NoC) has emerged as a cost-efficient and scalable architecture to solve the problem of high communication requests in traditional bus-based architectures [17,18]. The data transmission between Processing Elements (PEs) of NoCs is performed in the form of packets, where a packet is divided into multiple flow control units called Flits [6]. In the other words, packetized data is transferred between PEs in the form of flits using wires. During this transmission, the reliability of these flits may seriously be threatened by coupling capacitances between long and adjacent wires between PEs [1,22]. This phenomenon, called Crosstalk Faults, is among the main reliability challenges in NoCs [1]. With scaling down the technology size, the severity of crosstalk faults among wires is going to be further destructive in the future [22]. The main effects of crosstalk faults are: rising/falling delay, rising/falling speed-up and unwanted voltage glitches [28]. These effects can lead to: 1. misrouting and/or loss of the flits between the source and destination, 2. increasing the power consumption and, 3. degradation the performance of NoC-based systems [9]. Crosstalk faults severity depends on the transition patterns appearing on the wires [16]

Crosstalk faults tackling mechanisms can be applied at three different levels of design abstraction including: 1. physical level 2. transistor level [7,13] and, 3. Register Transfer Level (RTL) [5,7,8,10,11,15,23,26,27,29–31,34].

One drawback of physical and transistor level mechanisms is that they impose high overheads in terms of area overhead and timing to NoC-based systems [7]. At RTL, coding mechanisms can efficiently overcome the overhead problems in physical and transistor levels of design abstraction [34,7]. Among coding mechanisms, Crosstalk Avoidance Codes (CACs) can efficiently reduce the effects of crosstalk faults [21].

In CACs, crosstalk faults are reduced by preventing specific transition patterns. Based on the transition patterns that are prevented, CACs are categorized into Forbidden Overlapped Codes (FOCs) [4,34], Forbidden Transition Codes (FTCs) [7], Forbidden Pattern Free Codes (FPFs) [8,29,30,31,34] and One-Lambda Codes (OLCs) [34].

Among CACs, numeral-based OLCs are the most efficient types of coding mechanisms that can reduce the delay of crosstalk faults to its minimum possible value [34]. This is done by preventing the occurrences of opposite direction transitions while transiting between two consecutive flit transmissions. To reach this aim, the two transition

patterns 10→01 and 01→10 in tandem OLC code words are avoided. For example in NoC with 7 wires 1110000 is OLC code word but 10101010 is not. To generate OLC-based code words, two extra codec modules including the encoder and the decoder are required. These modules impose overheads in terms of area occupations, power consumption and critical path to the routers of NoCs. The mapping algorithm of numeral-based OLCs that maps data word to code word plays an important role on the overheads of codecs.

To find overhead-efficient numeral-based OLCs, this paper proposes a general Algorithm for Generating OLC Numeral systems (AGON). AGON can generate a collection of numeral-based OLCs. This can help designers in selecting efficient OLC-based numeral systems. Also, using AGON, an overhead-efficient numeral-based OLC called Subtraction-based-Numeral (Sub-Num) is generated. Sub-Num benefits two advantages: 1. it can omit OLC-induced transition patterns efficiently and, 2. it can reduce the overheads of codec more efficiently than other state-of-the-art OLC. Evaluation results using SPICE and VHDL simulations show that Sub-Num OLC can reduce power consumption and delay of wires by 10% and 9%, and also overheads of codec including dynamic power consumption, critical path and area occupation by 52%, 51% and 21%, respectively compared to the state-of-the-art numeral-based OLC.

The main contributions of this paper are as follows:

1. A general Algorithm for Generating OLC Numeral systems (AGON) is proposed.
2. Using AGON, a numeral system called Subtraction-based-Numeral (Sub-Num) is proposed. Experimental results show that Sub-Num outperforms other state-of-the-art OLC with respect to power consumption of codec, critical path of codec, area occupation of codec, delay and power consumption of wires.

The rest of this paper is organized as follows: Section 2 reviews the related work. Motivation is presented in Section 3. Section 4 proposes the AGON, and Section 5 proposes a numeral system called Sub-Num. Then, Sub-Num is evaluated in Section 6 and finally, conclusion remarks are given in Section 7.

2. Related work

Several mechanisms at different levels of design abstraction have been proposed in the literature to tackle crosstalk faults [4,5,7,8,10–12,23,29–31,33,34]. These mechanisms are proposed at three levels of design abstraction including: 1. physical level [33,26], 2. transistor level and, 3. Register Transfer Level (RTL) [4,5,8,10,11,23,29–31,34].

At physical level, mechanisms such as crosstalk-aware layout design [33] and shielding [21,35] can reduce crosstalk faults. In crosstalk-aware layout design, the amounts of the coupling capacitances are lessen by means of layout modification. In shielding mechanisms either in passive [21] or active types [35]; the coupling capacitances is reduced by inserting shield wires between the wires of NoC channels.

However, area overheads and high design costs discourage designers to utilize these mechanisms.

At transistor level, intentional time skewing prevents the occurrence of opposite direction transitions in adjacent parallel wires [7,13]. The skewing delay can be made by either a chain of inverters or a two-phase clock signal. Intentional timing skew is only applicable in repeater-inserted channels and imposes high overheads to NoC-based systems [29,35].

At RTL, coding mechanisms such as error control coding mechanisms and Crosstalk Avoidance Codes (CACs) [4,7,8,29–31,34] are proposed to tackle crosstalk faults. Error control coding mechanisms improve the reliability of NoC channels against crosstalk faults by increasing hamming distance between consecutive code words [7,10,11,23]. However, these mechanisms do not completely remove crosstalk faults from NoC channels and have limiting error detection and correction ability [21]. CACs forbid crosstalk-induced transition patterns to mitigate (or in some cases to eliminate) crosstalk faults from NoC channels. However, CACs have high complexity of their codec (encoder and decoder) modules, especially when the width of communication channel grows [7]. To solve this problem, numeral systems are among the efficient mechanisms. A numeral system is a mathematical notation for representing weight of code words by symbols in a consistent manner [7]. In the other words, numeral system is sequence of $\lambda_k\lambda_{k-1}, ...,\lambda_2\lambda_1$ symbols where λ_i determines the bases of ith numeral system and is used as a weight in representing code words. Forbidden Pattern Free Codes (FPFs) [8,29–31,34] Forbidden Overlapped Codes (FOCs) [4,34], Forbidden Transition Codes (FTCs) [7] and One-Lambda Codes (OLCs) [34] are different types of CACs based on classification of different transition pattern classes. Among these coding mechanisms, OLCs can more efficiently reduce the crosstalk faults by reducing the imposed delay to the victim wire in comparison with other CACs. However, with respect to this fact that numeral system plays an important role in the overheads of codec, an efficient mapping algorithm is required. In continue an efficient numeral-based OLC is proposed that can omit OLC induced transition patterns with cost-efficient overheads.

3. Motivations

According to the prediction of International Technology Roadmap for Semiconductors (ITRS), the number of PEs on a chip is increasing in coming years [20]. These huge numbers of PEs, require long, parallel and adjacent wires between them to communicate and send and receive data. This makes transferring data seriously prone to coupling capacitances between wires and generates crosstalk faults [19].

The increase of the crosstalk faults occurrences is serious in the future [1]. The rate of crosstalk faults increases proportional to the length of NoC wires [12]. It is predicted that the length of wires on chip would reach to 7000 $\frac{m}{cm^2}$ in 2020 [19]. Also, technology shrinkage affects the electrical parameters of wires in NoCs and increases the probability of crosstalk faults occurrences. Fig. 1 shows a sample of 5-bit wires with the electrical parameters. Where in this figure C_{iG} is load capacitance formed between a wire and the ground, C_{ij} and L_{ij} are the
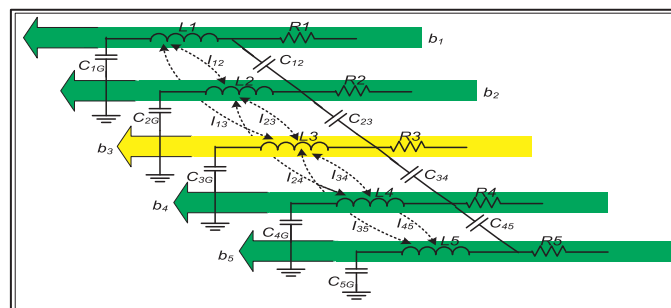

Fig. 1. A sample 5-bit wire and its electrical characteristics.