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Efficient one-dimensional forward and inverse discrete wavelet transformers

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ABSTRACT

This paper describes the efficient one-dimensional forward and inverse discrete wavelet transformers with 5/3 filter. This design reuses the same registers for both low-pass and high-pass filtering in different time slots. It utilizes 33% less registers, 17% less logic elements, has 7% higher maximum operating frequency and 2% lower total power dissipation than state-of-the-art filters.

1. Introduction

Discrete wavelet transform (DWT) is the foundation of JPEG 2000 still image compression standard, where the transform is the tool for image decomposition into multiple levels and subbands. The decomposed image consists of coefficients representing horizontal and vertical spatial frequency features of the original image [1]. The default one-dimensional (1-D) transformation into low-pass and high-pass coefficients is Le Gall's 5/3 filter [2].

JPEG 2000 standard supports both convolution-based and lifting-based filters. Convolution-based filters perform a series of multiplications and additions between low-pass and high-pass filter coefficients and pixels, extended at each image boundary [3–7]. The line-based architecture for DWT with reduced use of memory resources is presented in [8]. Main hardware architectures for DWT and their optimization techniques are reviewed in [9].

Lifting-based filtering consists of a sequence of alternative updating of pixels with odd indexes with weighted sum of pixels with even indexes, and updating of pixels with even indexes with weighted sum of pixels with odd indexes [10–18].

In directly mapped 5/3 filters with a single read port [10–11], the odd and even samples are read serially in alternate clock cycles and buffered, halving the overall pipelined filtering rate. This was solved by folding the last two pipeline stages into the first two stages [12]. The generalized programmable filter design is proposed in [13].

A hybrid of level-by-level and line-based DWT architecture was proposed in [14]. Pipelined architecture was presented in [15]. Highly efficient lifting-based DWT architecture utilizes parallel and folding processing in [16]. SIMD array architecture was proposed in [17]. The implementation that utilizes two systolic array filters and two parallel filters (systolic-parallel architecture) has been shown in [18].

An optimized adder-based 5/3 filter for low-area and low-power implementation is disclosed in [19]. The combination of parallel and pipeline techniques is disclosed in [20]. Parallel multilevel lifting-based DWT architecture was proposed in [21].

Our own previous research was disclosed in [22–26].

2. 1-D forward DWT

State-of-the-art 1-D forward DWT (Fig. 1) provides low-pass filtering $H_0(z)$ and downsampling by two, so output coefficients $y_0'[n]$ comprise even low-pass filtered coefficients $y_0[n]$. The same DWT also provides high-pass filtering $H_1(z)$ and downsampling by two, so output coefficients $y_1'[n]$ comprise even high-pass filtered coefficients $y_1[n]$.

The proposed 1-D forward DWT (Fig. 2) utilizes both even time slots for the generation of low-pass coefficients and odd time slots for the generation of high-pass coefficients.

Furthermore, the proposed 1-D forward DWT with Le Gall's 5/3 filter [2] utilizes the same registers (blocks with z^{-1} operators in Fig. 3) for the generation of both low-pass and high-pass coefficients in different time slots, by implementing low-pass transfer function $H_0(z)$ in even time slots and high-pass transfer function $H_1(z)$ in odd time slots. The switching between transfer functions $H_0(z)$ and $H_1(z)$ is performed by four switches controlled by the control signal c (Fig. 4).

Two upper switches are opened and two lower switches are closed for low level $c = 0$ and even input samples $x[n]$ ($n = 2k$). Two upper switches are closed and two lower switches are opened for high level $c = 1$ and odd input samples $x[n]$ ($n = 2k + 1$).

The equations describing internal filter signals in time instances from $n = 0$ to $n = 4$ are presented in Table 1.

Based on the equations for time instance $n = 4$, $y[n]$ can be expressed by equations (1) and, finally (2).

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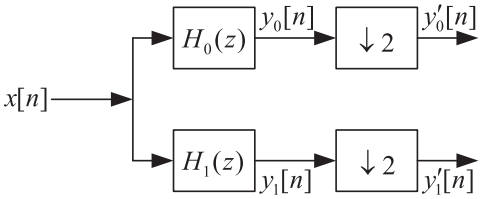

Fig 1. State-of-the-art 1-D forward DWT.

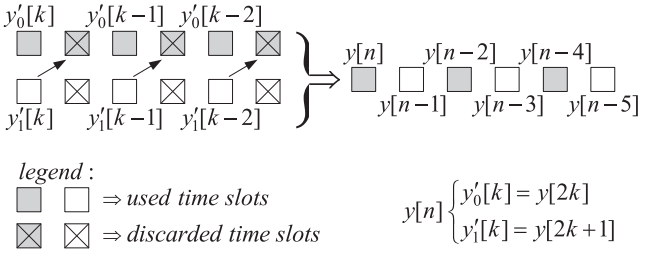

Fig 2. Time slots utilization.

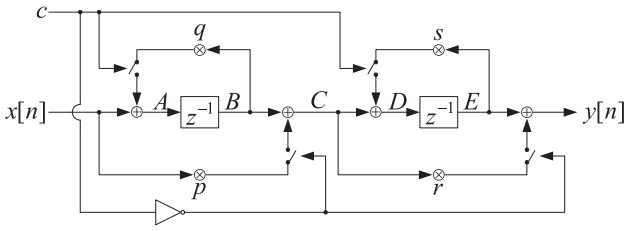

Fig 3. The proposed 1-D forward DWT with general multipliers.

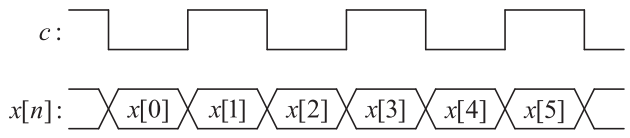

Fig 4. Control signal c timing.

From time instance $n = 4$, the processing is repeated in subsequent cycles.

Even output samples $y[n]$ are derived from the Eq. (2), which is appropriate to the Eq. (3) describing $H_0(z)$ in JPEG 2000 standard.

$$\begin{aligned} y[n] &= x[n-2] + p{\cdot}s{\cdot}x[n-2] + s{\cdot}x[n-3] \\ &\quad + q{\cdot}s{\cdot}x[n-4] + r{\cdot}x[n-1] \\ &\quad + r{\cdot}q{\cdot}x[n-2] + r{\cdot}p{\cdot}x[n] \end{aligned} \tag{1}$$

$$\begin{aligned} y[n] &= p{\cdot}r{\cdot}x[n] + r{\cdot}x[n-1] \\ &\quad + (1 + p{\cdot}s + q{\cdot}r){\cdot}x[n-2] \\ &\quad + s{\cdot}x[n-3] + q{\cdot}s{\cdot}x[n-4] \end{aligned} \tag{2}$$

$$\begin{aligned} y_0[n] &= -\frac{1}{8}x[n] + \frac{1}{4}x[n-1] + \frac{3}{4}x[n-2] \\ &\quad + \frac{1}{4}x[n-3] - \frac{1}{8}x[n-4] \end{aligned} \tag{3}$$

Eqs. (2) and (3) are identical for p, q, r and s derived from Eq. (4).

Table 1
Equations describing internal filter signals.

Time instance	Equations
$n = 0$	$A = x[n]$
$n = 1$	$B = x[n-1] = C$, $A = x[n] + q{\cdot}x[n-1]$
$n = 2$	$B = x[n-1] + q{\cdot}x[n-2]$, $A = x[n]$, $C = p{\cdot}x[n] + x[n-1] + q{\cdot}x[n-2] = D$
$n = 3$	$E = p{\cdot}x[n-1] + x[n-2] + q{\cdot}x[n-3] = y[n]$, $B = x[n-1] = C$, $A = x[n] + q{\cdot}x[n-1]$, $D = x[n-1] + p{\cdot}s{\cdot}x[n-1] + s{\cdot}x[n-2] + q{\cdot}s{\cdot}x[n-3]$
$n = 4$	$E = x[n-2] + p{\cdot}s{\cdot}x[n-2] + s{\cdot}x[n-3] + q{\cdot}s{\cdot}x[n-4]$, $C = x[n-1] + q{\cdot}x[n-2] + p{\cdot}x[n]$, $y[n] = E + r{\cdot}C$

$$\begin{aligned} 1 + p{\cdot}s + q{\cdot}r &= \frac{6}{8}, \\ p{\cdot}r &= -\frac{1}{8}, \\ q{\cdot}s &= -\frac{1}{8}, \\ r &= s = \frac{1}{4}, \\ p &= q = -\frac{1}{2} \end{aligned} \tag{4}$$

Odd output samples $y[n]$ are derived from the Eq. (5), which is appropriate to the Eq. (6) describing $H_1(z)$ in JPEG 2000 standard.

$$y[n] = p{\cdot}x[n-1] + x[n-2] + q{\cdot}x[n-3] \tag{5}$$

$$y_1[n] = -\frac{1}{2}x[n-1] + x[n-2] - \frac{1}{2}x[n-3] \tag{6}$$

Eqs. (5) and (6) are identical for p and q derived from the Eq. (7), which gives the same result as equations (4).

$$p = q = -\frac{1}{2} \tag{7}$$

The final proposed 1-D forward DWT (Fig. 5) is provided by inserting p, q, r and s from expressions (4) and (7) instead of general multipliers in Fig. 3, while four switches are realized as three multiplexers.

Input samples $x[n]$ are low-pass filtered within even time slots ($n = 2k$) without any need for downsampling by two, in order to produce even output samples $y_0[n]$ (3).

Input samples $x[n]$ are high-pass filtered within odd time slots ($n = 2k + 1$) without any need for downsampling by two, in order to produce odd output samples $y_1[n]$ (6).

Multipliers in the proposed 1-D forward DWT can be made as permanently shifted hard wired connections between output and input bit lines, thus avoid complex hardware multipliers.

Edge effects are avoided by symmetric extension of input samples at image boundaries, which is well known solution, or by dynamic change

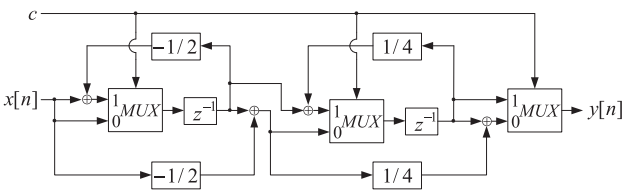

Fig 5. The proposed 1-D forward DWT with 5/3 filter.