



# Flicker modeling scheme of liquid crystal displays based on current leakage without information about TFT parameters

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## ABSTRACT

It is well known that the current leakage at a switching thin film transistor (TFT) of a pixel circuit is one of key factors for the luminance fluctuation of liquid crystal displays (LCDs) perceived as a flicker artifact. This paper proposes a flicker estimation scheme based on the current leakage model of an amorphous silicon (a-Si) TFT. The proposed scheme consists of four blocks such as gray-to-voltage conversion, pixel voltage update, voltage-to-transmittance conversion, and flicker estimation. Gray-to-voltage and voltage-to-transmittance conversion blocks are built from measured data at a source driver and a panel for gray levels. Flicker estimation is established by applying fast Fourier transform (FFT) to simulated transmittance waveforms. The pixel voltage update block is made up by the voltage leakage model which parameters are estimated by matching simulation results to measurement results at a band gray pattern regarding several gray levels. Any given information of TFTs is not required for parameter extraction. The proposed method is applied to a WSXGA+ in-plane switching (IPS) LCD of a 1-dot inversion and flicker levels are estimated within an error range of  $\pm 0.6$  dB at full gray patterns of gray levels from 32 to 224, compared to measurement results.

## 1. Introduction

Flicker takes place from the luminance fluctuation caused by the periodic refresh of a display. This fluctuation becomes a serious perceptible artifact when its amount is large to some level compared to the average value based on Weber's law and its frequency is lower than the critical flicker frequency (CFF) according to the temporal contrast sensitivity function (TCSF) of human beings [1,2]. Especially, in liquid crystal displays (LCDs) many studies have been conducted to analyze and reduce the visible flicker caused by various factors such as insufficient charging time, large kickback voltage, dithering algorithm, backlight scanning, backlight dimming, and leakage current at a switching thin film transistor (TFT) of a pixel circuit [3–11].

In the area of flicker analysis and modeling, the lowest refresh frequency of a flicker-free display has been referred to as CFF and its prediction model has been proposed as a function of the natural logarithm with refresh rates and sizes of cathode ray tube (CRT) displays for a theoretical standard observer [13]. Meanwhile, the switching TFT in a pixel has been investigated for its effect on flicker [3]. Three types of low temperature poly silicon (LTPS) TFTs are evaluated with different mobility, overlap capacitance, and leakage current. Instead of optical

flicker, the electrical flicker has been estimated over the fluctuation of the pixel voltage, which reached the conclusion that the leakage current is the most critical factor causing the resultant flicker. Some previous studies have been conducted about the relation between motion blur and flicker in impulse-type displays [4] and the dimming flicker in adaptive dimming low power LCDs [5,11].

For the flicker reduction, the inter-modulation between the refresh frequency of a panel and the pulse width modulation (PWM) frequency of a backlight has been sifted through for flicker visibility and the optimum PWM modulation frequency has been extracted at a given refresh rate for flicker-free LCDs [6]. It has been reported that dithering patterns that are utilized to increase the perceptual bit depth of gray scales could cause flicker. By selecting appropriate dithering patterns with consideration of polarities of pixels, flicker has been ameliorated [7]. The coupling of backlight driving signals to pixel electrodes can increase flicker level and the automatic delay adjustment has eliminated artifacts [8]. On the other hand, the reduced difference between positive and negative transmittance and the lower leakage current have improved flicker by adopting new liquid crystal material and oxide TFTs, respectively [9,10]. Flicker has been also reduced by using control signals of different voltage ranges for positive and negative pixel

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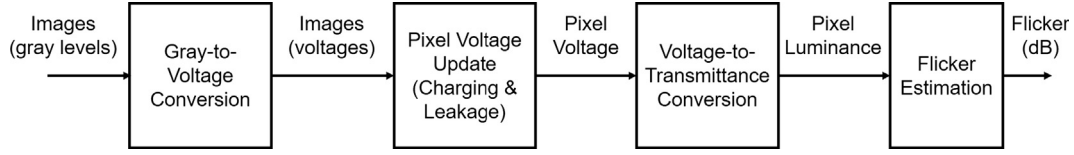


Fig. 1. Overall architecture of flicker estimation.

voltages [12].

This paper focuses on the flicker estimation based on the current leakage equation of an amorphous silicon (a-Si) TFT. Unlike the previous approach using actual TFT parameters and the fluctuation of electrical pixel voltage [3], an optical flicker model is established based on measured flicker levels under several conditions of test patterns and gray levels without any information about TFT parameters.

## 2. Proposed flicker estimation scheme for LCDs

The overall architecture of a proposed flicker estimation is shown in Fig. 1 for LCDs. First, gray levels of input patterns are converted to corresponding voltages based on the gray-to-voltage curve of a given LCD panel. These converted voltages are programmed into pixels line-by-line with consideration of charging and leakage operations. If the pixel is placed in the current driving line, the pixel is charged with the programming voltage. Otherwise, the pixel voltage is adjusted by taking into account the leakage between the pixel electrode and the column line. It is assumed that the pixel charging time is long enough compared to a time constant of resistive and capacitive loads. Then, the pixel voltages in line times are transformed into the pixel transmittance that is directly proportional to the luminance in LCDs. Finally, the resulting flicker level is estimated from the transmittance waveform by means of fast Fourier transform (FFT) and TCSF.

To obtain the gray-to-voltage curve of a panel, the voltage is measured directly at the output of a source driver circuit. Because a test panel is driven in a way of 1-dot inversion, the output voltage for a full gray pattern of one gray level has an equivalent shape to Fig. 2 which positive and negative voltages can be extracted from. The active region is driven at the line frequency for a given gray level and the vertical blank period is driven at a black level. Finally, the resultant gray-to-voltage curve is established with half of the difference between positive and negative voltages by assuming that a common voltage ( $V_{COM}$ ) is zero.

To emulate a real panel operation, column lines of a panel are updated with converted pixel voltages every line time. In (1),  $V_f(m)$  is the  $m$ -th image converted in voltage and  $V_{col}(n, c, m)$  is the voltage of the  $c$ -th column at the  $n$ -th line and the  $m$ -th frame where  $HRES$  is a horizontal resolution and  $VTOTAL$  is the sum of a vertical resolution and a vertical blank.

$$V_f(m) = \{V_{col}(n, c, m) | 1 \leq n \leq VTOTAL, 1 \leq c \leq 3 \times HRES\} \quad (1)$$

$$V_{pix}(y, c, t) = \begin{cases} V_{col}(n, c, m) & \text{if } y = n \\ V_{pix}(y, c, t-1) - \Delta V & \text{otherwise} \end{cases}$$

where  $1 \leq y \leq VRES$ , and  $t = n + (m-1) \times VTOTAL$  (2)

Overall pixel voltages  $V_{pix}(y, c, t)$  are updated every line time regarding the column voltage as described in (2) where  $VRES$  is a vertical resolution and  $t$  is the operating time in a unit of line time. When columns are driven for the  $n$ -th line of the image, pixels of the corresponding line are directly programmed by column voltages and voltages of other pixels are changed by the current leakage of switching TFTs. In (2),  $\Delta V$  is the voltage variation due to the current leakage during one line time.  $\Delta V$  of the proposed flicker model is calculated based on the current leakage equation of a Rensselaer Polytechnic Institute (RPI) amorphous silicon TFT model that is described in (3) [14]. While  $IOL$ ,  $VDSL$ ,  $VGSL$ , and  $SIGMA0$  are constant parameters,  $V_{GS}$  and  $V_{DS}$  are gate-source and drain-source voltages of a switching TFT. In the proposed scheme, the second and third terms of (3) are ignored by assuming that the exponential term of  $V_{DS}$  would be dominant. In addition,  $\Delta V$  is obtained with a line time ( $T_{Line}$ ) and a pixel capacitance ( $C_{pix}$ ) including storage and liquid crystal (LC) capacitors as expressed in (4). The resultant voltage leakage equation is given as (5) that requires three parameters of  $VOL$ ,  $VDSL$ , and  $VGSL$  in conjunction with  $V_{GS}$  and  $V_{DS}$ . The extraction scheme of these three parameters is dealt with in Section 3.2.

$$I_{leakage} = IOL \cdot \exp\left(\frac{V_{DS}}{VDSL}\right) \cdot \exp\left(-\frac{V_{GS}}{VGSL}\right) - IOL \cdot \exp\left(-\frac{V_{GS}}{VGSL}\right) + SIGMA0 \cdot V_{DS} \quad (3)$$

$$\Delta V = \frac{I_{leakage} \cdot T_{Line}}{C_{pix}} \quad (4)$$

$$\Delta V \approx VOL \cdot \exp\left(\frac{V_{DS}}{VDSL}\right) \exp\left(-\frac{V_{GS}}{VGSL}\right) \quad (5)$$

The estimated pixel voltages are used to calculate the transmittance of all pixels at each time step of a line time by means of LC response model and voltage-to-transmittance curve [15–17]. For the output LC voltage response ( $V_{LC}(n)$ ) and the input pixel voltage ( $V_{pix}(n)$ ), the step response ( $S_{LC}(n)$ ) is given by (6) based on an equivalent circuit model

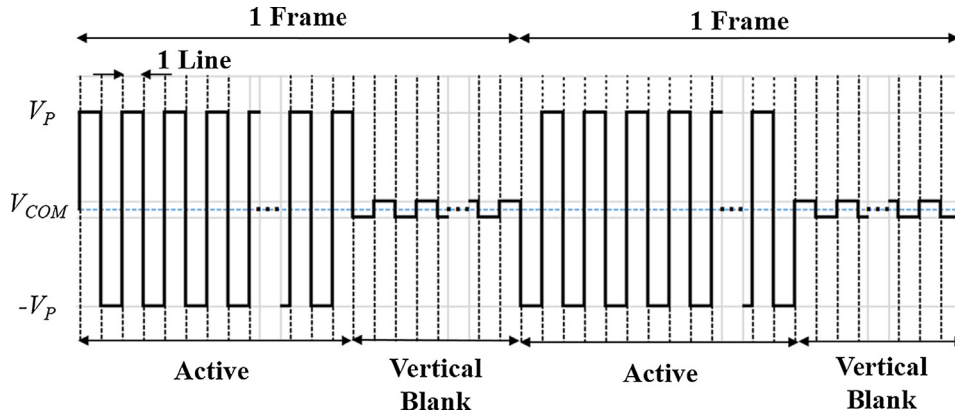


Fig. 2. Output voltage waveform of a source driver at a full gray image.

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