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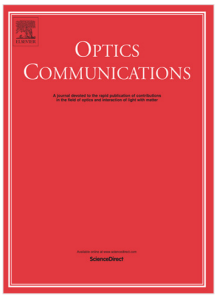

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Subhradeep Pal, Sumanta Gupta

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Performance Analysis of an Electrostatic Doping Assisted Silicon Microring Modulator

Subhradeep Pal[a], Sumanta Gupta[a,*]

[a]*Department of Electrical Engineering, Indian Institute of Technology Patna, Bihta, Bihar-801106, India.*

Abstract

In this paper, we propose and numerically analyze electrostatic doping (ED) assisted silicon microring modulator (MRM) realizable on SOI platform having ∼ 10 nm free spectral range (FSR). The proposed modulator consists of a vertical metal-insulator-semiconductor (MIS) junction and a lateral metal-semiconductor (MS) junction. It utilizes ED to achieve free carriers inside the rib waveguide that eventually introduces the free carrier plasma dispersion effect. The proposed device does not employ any lateral or vertical PN or PIN junction and offers high operating speed with negligible static power consumption. Numerical simulation using commercially available TCAD tools and mode solvers are used to estimate the performance of the proposed modulators. Palladium (Pd) and aluminum (Al) are used as electrodes to realize ED enabled MIS-MS charge plasma diode. The performance of the proposed modulator is extensively studied both in steady state and transient state. Results predict that a maximum 37.8 dB and 33 dB of extinction ratio (ER) is achievable by the modulator while operating in inversion and accumulation mode, respectively. Predicted insertion losses are 1.97 dB and 1.49 dB when operated in inversion and accumulation mode respectively. The proposed modulator is expected to provide a maximum of 26.3 Gbps and 32.2 Gbps operating speed with a 9.21 GHz and 11.9 GHz of 3-dB optical bandwidth in inversion and accumulation mode of operation, respectively. Simulation result predicts that the dynamic energy per bit for the proposed ED assisted MRM is approximately 31 fJ/bit and 68 fJ/bit in inversion and accumulation mode of operation, respectively.

Keywords: electrostatic doping, microring modulator, work-function, plasma dispersion effect, intensity modulator.

1. Introduction

Optical or photonic interconnects offering higher bandwidth with lower power consumption are slowly replacing the copper counterparts in next generation data centers and telecommunication industries [1, 2]. For a sustainable growth for the photonic interconnects, the operational and production cost has to be reduced below than that of Cu counterpart while delivering superior performance [3]. Silicon photonics is a potential solution to this problem since it employs the mature CMOS fabrication technology which supports device scaling. In the present scenario, there is a very high demand for ultra-small silicon photonic modulators suitable for intra-chip communication or short reach optical links especially in the data-center industry [4, 5, 6]. With the help of mature CMOS fabrication technology, next-generation ultra-small silicon photonic devices are expected to offer extremely low power consumption in the order of 10 fJ/bit or less [7, 8]. To reduce the device dimensions and power consumption we need to scale down the device which is very common in CMOS technology. This can be achieved by increasing the doping concentration of the device layer [9, 10]. However, with reducing device dimensions random dopant fluctuations (RDF) [11, 12] or unreliable doping concentrations [9, 10] along with unintentional and undesired ionized dopants in the active region of the device impose serious challenges to fabricate any nano-scale device and PICs with high yield [13]. In this respect use of electrostatic doping (ED) can be an alternative solution to cope up with these problems. Electronic devices based on ED like doping less diode [13, 14], transistor [15], nanowire transistor [16] have been proposed and analyzed in the past. The primary advantage of ED is that it can introduce different types of carriers (both electrons and holes) electrically by creating an accumu-

*Corresponding author: Dr. Sumanta Gupta
Email addresses: subhradeep.pee13@iitp.ac.in (Subhradeep Pal), sumanta@iitp.ac.in (Sumanta Gupta)