



Reconfigurable VLSI design of a changeable hybrid-radix FFT hardware architecture with 2D-FIFO storing structure for 3GPP LTE systems

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Abstract

This paper presents a reconfigurable Fast Fourier Transform (FFT) hardware architecture for 3GPP LTE systems. In the main FFT computing process, a novel processing kernel engine is proposed to support four configuration types of changeable hybrid-radix FFT operations. Also, in the data storage manipulation, a smart 2D-FIFO structure is used to flexibly handle efficient reading/writing data access for 36 different FFT sizes. In addition to a field-programmable gate array prototyping design approach, we provide application-specific integrated circuit implementation via TSMC 90-nm CMOS technology. The developed FFT chip only occupies a core area of 1.416 mm², consumes 24.2 mW of power, and reaches maximum speed of 111.11 MHz.

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Keywords: Reconfigurable; Hybrid radices; 2D FIFO; Fast Fourier transform; 3GPP LTE

1. Introduction

Over the past decades, Fast Fourier Transform (FFT) has become a popular design approach in fields ranging from algorithm domain analysis to hardware development. In many circuit implementations, single-path delay feedback [1] based architecture is considered a popular design approach to realize FFT functions. Initially, FFT focused only on single-radix manipulation [2–4]. Recently, research has shown a trend toward multiple-radix processing [5–7]. The approach in [5] simply utilized duplicate computing paths to accomplish the different radices of FFT, causing large hardware overhead and power/energy waste. In addition, [6] and [7] only presented several basic FFT modes defined in 3GPP LTE systems. Instead, we want to develop a reconfigurable FFT hardware architecture that supports as many FFT modes as possible and achieves both increased hardware and energy efficiency.

The rest of this paper is organized as follows. Section 2 presents the proposed hardware architecture. Section 3 shows both field-programmable gate array (FPGA) prototyping and application-specific integrated circuit (ASIC) implementation. Section 4 includes the design chip comparison, while Section 5 concludes.

2. Proposed hardware architecture

2.1. Proposed reconfigurable hardware architecture

Fig. 1 indicates various FFT modes defined in 3GPP LTE systems. The predefined FFT sizes vary in accordance with different combination of (X , Y , and Z). The maximum FFT size supported is 2048 FFT-points ($X = 11$, $Y = 0$, and $Z = 0$). Therefore, we want to develop a reconfigurable FFT hardware architecture, as depicted in Fig. 2. In the main FFT-computing, a novel reconfigurable processing kernel engine (R-PKE-4) is proposed to support four types of configuration, which can execute changeable hybrid-radix FFT operations. As for data storage, a smart two-dimensional (2D) FIFO structure

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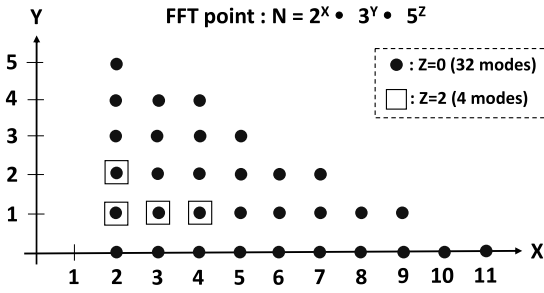


Fig. 1. FFT mode definition in 3GPP LTE systems.

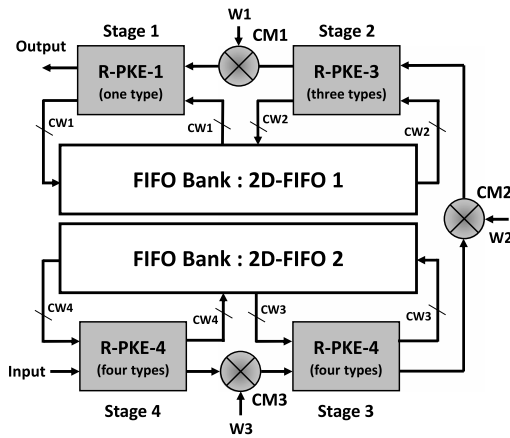


Fig. 2. Block diagram of proposed FFT hardware architecture.

is developed to flexibly realize easy data-reading/writing access for 36 different FFT modes.

2.2. Four types of radix-5 based reconfigurable processing kernel engine

In the main FFT operation portion, we propose a reconfigurable processing kernel engine (R-PKE), which is highly based on radix-5 FFT-computing, as illustrated in Fig. 3. This design feature performs changeable hybrid-radix computation on this engine without any extra circuit overhead of complex multipliers and adders. By making good use of the hardware reuse property, R-PKE (also called R-PKE-4) can be changed into four types of configuration, realizing different combined radices as follows.

- (1) Type A (TA): radix-5 processing.
- (2) Type B (TB): radix- 3^i processing ($i = 1$ or 2).
- (3) Type C (TC): radix- 2^j processing ($j = 1, 2$ or 3).
- (4) Type D (TD): concatenated radix-3 and radix-2 processing in series.

As shown in Fig. 3, TA_S1_In1 to TA_S1_In4 indicate four input signals from the first to fourth FIFOs of substage 1, respectively, while R-PKE-4 is considered as “Type A” processing. In “Type B” processing, two output signals to two FIFOs in substage 2 are denoted as TB_S2_Out1 and TB_S2_Out2. Other signal notations are deduced in an analogous manner. The crucial hardware circuit includes four complex multipliers and eighteen complex adders in total, which are grouped into ten groups, B1–B10. The hardware resource utilization for different configuration types is denoted by different colors. Furthermore, the computing elements in B5 are not activated

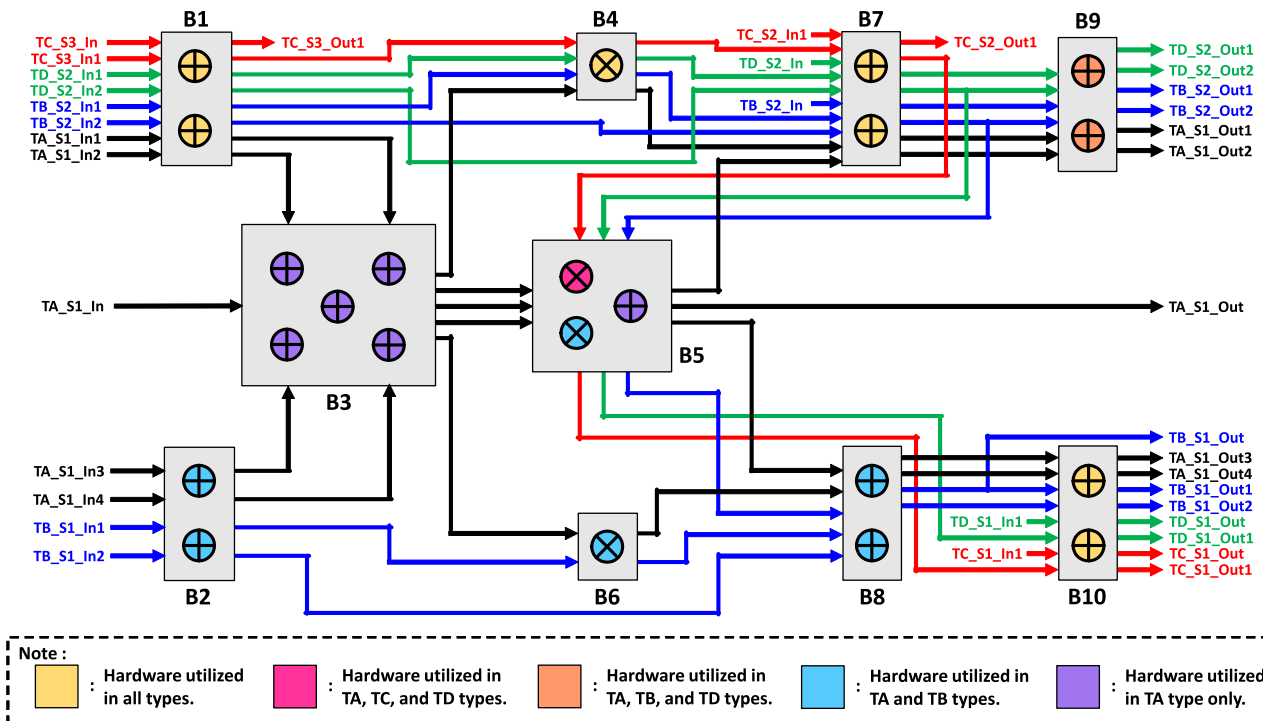


Fig. 3. Block diagram of proposed 4-type radix-5 based reconfigurable processing kernel engine (R-PKE-4).

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