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A CMOS, low-power current-mirror-based transimpedance amplifier for 10 Gbps optical communications

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ABSTRACT

In this paper, a new low-power CMOS optical transimpedance amplifier (TIA) for 10 Gbps applications is proposed. The main objective of this work is to achieve low-power consumption while meeting other required performances. The input resistance is considerably decreased due to the use of diode-connected input stage at the input node. Moreover, the output node benefits from an active inductive peaking technique which is used as the output load to extend the frequency bandwidth while keeping the low-power performance of the proposed TIA. Moreover, the core amplifier uses no passive elements which leads to a small chip area. Furthermore, to verify the performance of the proposed TIA, the circuit simulations are done in HSPICE using 90 nm CMOS technology parameters. So, the simulation results show the transimpedance gain of 40.5 dbΩ, -3 dB frequency bandwidth of 7 GHz, input referred noise of 20.3pA/$\sqrt{Hz}$ and the power consumption value of only 1.4 mW at 1 V supply. Finally, other simulation results such as Monte-Carlo analysis, eye diagram and noise analysis justify the proper performance of the proposed TIA which can be operated as a low-power building block in a 10 Gbps optical receiver system.

1. Introduction

Due to the current advances in the communication systems and the growing demands for high-speed data rates, fiber optic communications system (which uses the light beam as a carrier signal) attracted more and more attention in the recent years. However, the modulated data on a beam of light needs to be converted back to an electrical signal at the front-end part of the optical receiver which should provide a wide frequency bandwidth, proper peak to peak output swing and low value of the input referred noise. That is why the Transimpedance Amplifier (TIA) stage in the front-end plays an essential role not only for converting the photodiode's output current signal to the voltage form, but also, amplifying the weak photodiode output current to provide a proper signal quality for the subsequent digital signal processing stages. Fig. (1a), shows the block diagram of an optical receiver system and Fig. (1b) shows the block diagram of a low noise optical receiver which uses a replica TIA to properly eliminate the noise of the main TIA as a common mode voltage in the differential Limiting Amplifier (LA) stage at the cost of higher power consumption.

Giving the above facts, proper design of the TIA stage as one of the most critical building blocks in an optical receiver system is a challenging and time-consuming task, due to the fact that, the designer should consider the design trade-offs between the design performances such as transimpedance gain, frequency bandwidth, input referred noise and power consumption values for the required bit-error-rate. So, the design of a low-power optical receiver system is a complex multi-objective optimization problem. However, due to the low chip area as well as fabrication cost and high integration density besides low-power consumption characteristic; CMOS technologies are widely-used for fabrication of optical receiver ICs in comparison with other semiconductor materials such as GaAs and InP [1,2].

On the other hand, one of the most challenging issues in designing high-frequency TIA stages is the dominant pole frequency which is the main reason of the bandwidth limitation at the input node, due to the large parasitic capacitance of the photodiode. So, in addition to the main trade-offs exist in the design of analog circuits between gain, bandwidth, voltage headroom, noise and power consumption, the effect of large photodiode capacitance at the input node makes the design of TIA stages even more challenging.

Furthermore, using passive inductive peaking technique is an

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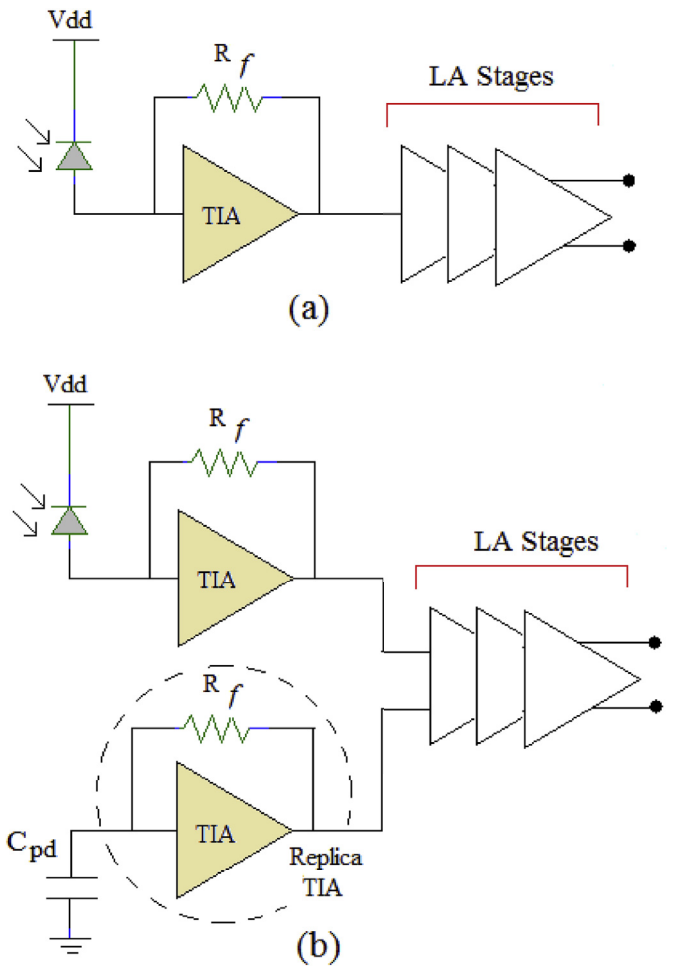

Fig. 1. (a) Block diagram of an optical receiver system, (b) A low-noise optical receiver structure.

effective method for bandwidth enhancement [3,4] but, at the cost of larger occupied chip area. In addition, Regulated Cascode (RGC) topology is widely used in the design of TIA circuits due to the fact that RGC structure is an improved version of common gate topology which alleviates the effect of photodiode parasitic capacitance to some extent. So, less input resistance and higher frequency bandwidth are expected using RGC topology. On the other hand, the RGC topology cannot provide a proper noise performance in comparison with the common-gate topology [5].

However, some TIA structures are discussed in the previously published literature [6–14]. In Ref. [6], an inductor-less inverter-based TIA with active common-drain feedback is presented which shows a higher gain performance in comparison with the conventional RGC topology. But, the circuit suffers from the existence of a parasitic miller capacitance at the input node which limits the frequency bandwidth of the TIA circuit. In Ref. [7], instead of using an N-well/P-substrate junction in CMOS-compatible photo detectors (CMOS-PD), a P^+/N-well junction is used to improve the speed of the receiver, but, a high number of resistors are used in the design, which requires large chip area. In Ref. [8], to obtain a proper gain value, three stages of cascaded inverters are employed while, a passive inductive series peaking technique is used to extend the frequency bandwidth which itself demands a considerable occupied chip area. Moreover, as it is discussed in Ref. [9], by using a common source transistor as a voltage-current feedback, the input and output impedances are properly reduced, but, the compensation inductors are also used to achieve a proper frequency bandwidth at the cost of large occupied chip area.

On the other hand, the noise challenge is another complex aspect of designing high performance TIAs which requires to be considered carefully especially for applications beyond 10 Gbps. In Ref. [10], capacitive matching technique based on the method discussed in Refs. [4,11] is used, which shows unfavorable noise behavior.

However, as it is discussed in Refs. [12,21,28], using series peaking technique at the input node is another solution to decrease the effect of the input capacitance as well as the noise value at higher frequencies. But, using passive inductors occupies a large chip area. Moreover, in Ref. [13], a low-noise, two-stage, front-end (TSFE) structure is proposed which combines a narrow bandwidth TIA at the first stage with an equalizer at the second stage, to obtain a low-noise behavior in an extended bandwidth at the price of high-power consumption, and in [20], a compression stage is proposed using inverter strcuture, which benefits from a wide dynamic range.

Giving the above facts, the main focus of this work is to reduce the power consumption of the TIA circuit, and the low-power TIA is designed in 90 nm CMOS technology for 10 Gbps applications. However, in order to reduce the chip area, an active inductive peaking technique is used to provide an extended frequency bandwidth while consuming lower value of power. Moreover, to overcome the noise problem, a feedback network is considered in the TIA circuit as it is shown in Fig. (1-b).

So, this paper is organized as follows: In section 2, the proposed TIA circuit is presented and discussed in details. In section 3, the simulation results of the proposed TIA structure are presented. In Section 4, the noise analysis of the proposed TIA based on the TIA's noise equivalent circuit model is presented and finally, the conclusions are presented in section 5.

2. The proposed TIA

The proposed TIA circuit topology and the open-loop small signal equivalent circuit model of the TIA are shown in Figs. (2) and (3), respectively. The weak current signal generated by the photodiode is amplified in three steps as follows:

First, the weak current signal of photodiode is amplified proportional to $\left(\frac{W2}{W1}\right)$ to generate i_{o2}, then, the current at the drain of M_2 is amplified by a factor of $\left(\frac{W4}{W3}\right)$ to generate i_{o4} and finally, i_{o4} is multiplied by a factor of $\left(\frac{W6}{W5}\right)$ to reach the output node.

So, the open-loop transimpedance gain at the mid-band frequencies (A_R) can be written as follows:

$$A_R = \frac{V_{out}}{I_{in}} = \frac{1}{g_{m1}} \cdot g_{m2} \cdot \frac{1}{g_{m3}} \cdot g_{m4} \cdot \frac{1}{g_{m5}} \cdot g_{m6} \cdot \frac{1}{g_{m7}} = \left(\frac{\left(\frac{w}{L}\right)_2}{\left(\frac{w}{L}\right)_1} \times \frac{\left(\frac{w}{L}\right)_4}{\left(\frac{w}{L}\right)_3} \times \frac{\left(\frac{w}{L}\right)_6}{\left(\frac{w}{L}\right)_5} \right) \cdot \frac{1}{g_{m7}} \quad (1a)$$

In which, I_{in} is the input current of the TIA, g_m is the transconductance, W is the width and L is the length of a MOSFET transistor.

However, by assuming equal channel length (L) for all transistors, the following result is obtained:

$$A_R = \left(\frac{W_2}{W_1} \times \frac{W_4}{W_3} \times \frac{W_6}{W_5} \right) \cdot \frac{1}{g_{m7}} \quad (1b)$$

In order to obtain an extended frequency bandwidth, it is necessary to reduce the input resistance without the requirement of consuming higher power value. However, due to the diode-connected transistor (M_1) used at the input node, the input resistance value in the proposed circuit is quite low which is equal to $(g_{m1})^{-1}$. Moreover, as it is shown in Fig. (2), a voltage-current feedback network (R_f) is used to decrease the value of the input and output resistances, so, the poles associated with these nodes are moved to higher frequencies, which results in an extended frequency bandwidth.