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A CMOS symmetric self-biased voltage reference

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ABSTRACT

This paper presents a novel CMOS voltage reference circuit named symmetric self-biased voltage reference (SSVR), which enables not only to discard the voltage headroom issue of a conventional constant-g_m current source and the inevitable need of an extra bias in a modified constant-g_m current source, but also to maintain stable bias voltages with strong tolerance against significant variations of power supply and temperature. Test chips of the SSVR were implemented by using a 0.11-μm CMOS process. Measured results demonstrate that the symmetric configuration of the proposed SSVR helps to achieve constant voltage references against the V_{DD} variation from 0.7 to 1.2 V and the temperature variation from −15 °C to 125 °C. The fabricated chip consumes constant 18.5 μA currents for 0.7 ~ 1.0-V supply voltages and its core occupies the area of $0.04 \times 0.047\ mm^2$.

1. Introduction

CMOS VLSI systems have been rapidly proliferated for the past decades, and its supply voltages have been scaled down below 1.2 V since the channel-length has been narrowed to tens of nano-meters. Accordingly, a number of studies have been conducted to examine the feasibility of analog and digital integrated circuits with a sub-1 V supply voltages [1,2].

In particular, stable bias circuits such as low dropout (LDO) voltage regulators have become crucial for CMOS VLSI systems. As shown in Fig. 1, a typical LDO requires a voltage reference that needs to be stable over significant PVT variations (usually occurred in mixed-signal integrated circuits). Also, the error amplifier mandates stable current sources. Otherwise, the output voltages would be severely deterred and noisy [3]. Therefore, circuit designers must provide a novel voltage reference circuit which not only equips strong tolerance characteristics against voltage and temperature variations, but also enables to operate with a sub 1-V supply voltage for low power consumption.

For this purpose, stable reference circuits have been numerously investigated. Among various bias configurations, a basic current source is a current-mirror which is yet vulnerable to the channel-length modulation effect of MOSFETs and is likely to generate considerably unstable DC currents. Then, a cascode current-mirror was suggested to alleviate this channel-length modulation effect [4,5]. However, it suffers significant voltage headroom issue, thus limiting its usage for low voltage operations.

Hence, a modified cascode current-mirror was developed to discard the voltage headroom issue [4]. However, it still needs an extra bias voltage to operate (which will be covered in Section 2–2.2). In this paper, we propose a novel symmetric self-biased voltage reference (SSVR) by applying this modified cascode current-mirror circuit technique to a well-known conventional constant-g_m current source.

Section 2 describes the operation mechanism of the conventional constant-g_m current source and its modified circuit, and of the proposed SSVR. Section 3 demonstrates the measured results of the SSVR. Then, conclusion is followed.

2. Circuit description

2.1. Conventional constant-g_m current source(C-CGCS)

Fig. 2 shows the schematic diagram of a conventional constant-g_m current source (C-CGCS) that utilizes four NMOSs, two PMOSs, and a precision resistor (R_{PRE}). As aforementioned, its cascode structure inhibits its usage for low supply voltages because of the large voltage headroom. Namely, the minimum drain voltage (V_{D3}) of Q_3 is given by,

$$V_{D3,\min} = V_{tn} + 2V_{OV,n}, \quad (1)$$

where $V_{OV,n}$ and V_{tn} represent the overdrive voltage and the threshold voltage of an NMOS, respectively.

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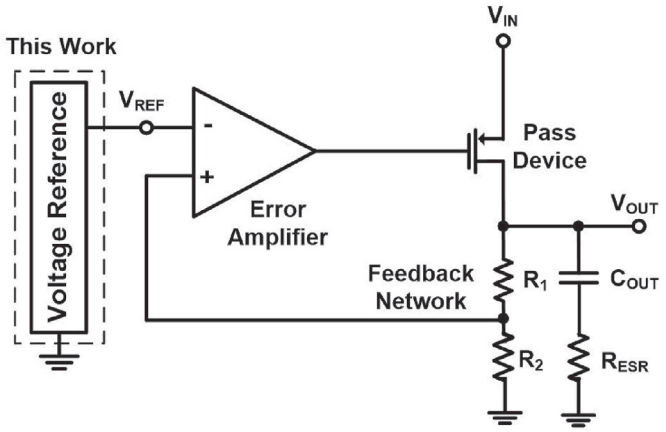

Fig. 1. Block diagram of a typical LDO.

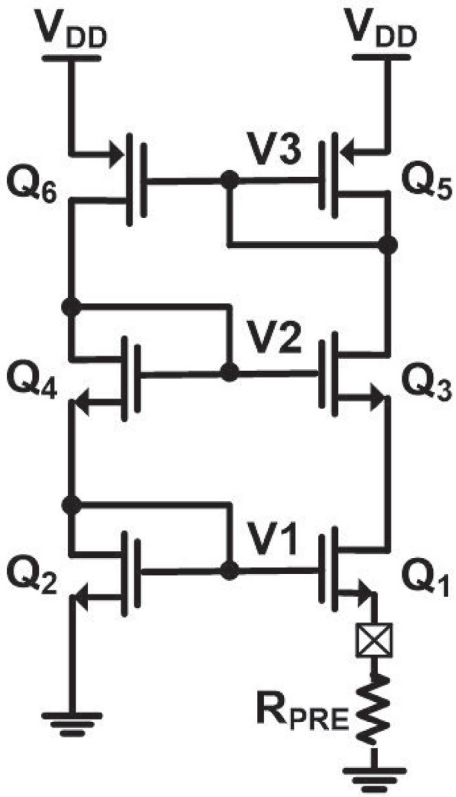

Fig. 2. Schematic diagram of the conventional constant-g_m current source.

It is certainly difficult to lower the supply voltage (V_{DD}) down to a sub 1 V in this configuration, because

$$V_{DD,\min} = V_{tn} + 2V_{OV,n} + |V_{tp}| + |V_{OV,p}| = 2V_{tn} + 3V_{OV,n}, \quad (2)$$

where $|V_{OV,p}|$and $|V_{tp}|$represent the overdrive voltage and the threshold voltage of a PMOS. For simplicity, it is assumed that $V_{OV,n} = |V_{OV,p}|$and $V_{tn} = |V_{tp}|$.

2.2. Modified constant-g_m current source (M-CGCS)

Fig. 3 depicts the modified constant-g_m current source (M-CGCS) which exploits the modified NMOS cascode circuit to alleviate the voltage headroom issue of the C-CGCS [6]. Thereby, the M-CGCS can lower the supply voltage (V_{DD}) down to a sub 1 V while maintaining stable performance. It is clearly seen that the drain voltage (V_{D4}) of Q_4 is

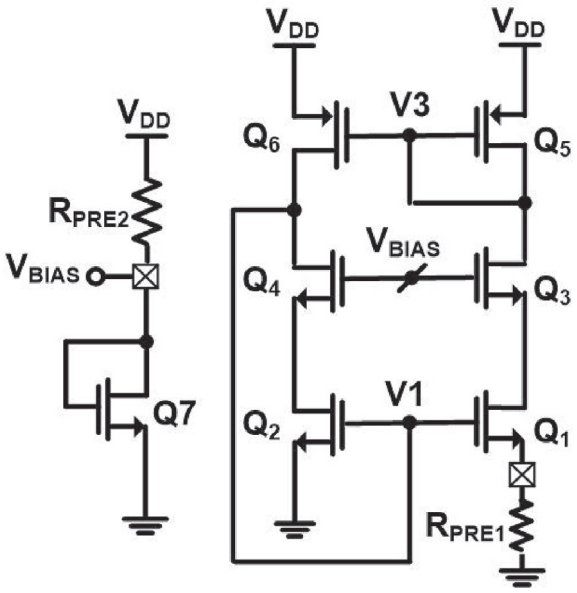

Fig. 3. Schematic diagram of the modified constant-g_m current source.

the same as $V_{GS,2}$, and also that the bias voltage (V_{BIAS}) maintains the value of (V_{tn} + $2V_{OV,n}$) to keep Q_4 operating in saturation. Hence, the minimum drain voltage ($V_{D3,\min}$) of Q_3 can be lowered down to $2V_{OV,n}$.

In consequence, this M-CGCS can lower V_{DD} than the C-CGCS, i.e.,

$$V_{DD,\min} = 2V_{OV,n} + |V_{tp}| + |V_{OV,p}|. \quad (3)$$

However, the modified constant-g_m current source shows an inherent disadvantage which is the need of an extra bias voltage (V_{BIAS}) for the gates of Q_3 and Q_4. An extra transistor (Q_7) and a precision resistor should be added. The aspect ratio $(W/L)_7$ of Q_7 should be designed to be 1/4 times $(W/L)_2$ of Q_2 to generate V_{BIAS}, thus leading to 1/4 times small DC-current flow.

2.3. Symmetric self-biased voltage reference(SSVR)

Fig. 4(a) shows the well-known temperature compensation property of diode-connected NMOS and PMOS transistors, in which a diode-connected NMOS demonstrates the tendency of complementary-to-absolute temperature (CTAT) and a diode-connected PMOS yields the characteristics of proportional-to-the-temperature (PTAT). Therefore, the symmetric topology with a pair of diode-connected NMOS and PMOS transistors can be exploited as a stable voltage reference against the considerable temperature variation from −15 °C to 125 °C.

By utilizing this property, we propose the symmetric self-biased voltage reference (SSVR) in this paper, which removes the need of an additional bias circuit and enables sub 1-V operations. It can be applied to versatile analog circuits such as operational amplifiers, LDOs, etc. Fig. 4(b) depicts the feasible reference voltage of the SSVR, in which the diode-connected PMOS-cascode shows PTAT characteristic whereas the NMOS-cascode provides the tendency of CTAT. Hence, the final SSVR can generate stable reference voltages against the temperature variations from −15 °C to 125 °C [7].

Fig. 5 shows the schematic diagram of the SSVR, where the modified NMOS cascode circuit ($Q_1 \sim Q_4$) is exploited and a PMOS modified cascode configuration ($Q_5 \sim Q_8$) is built above the NMOS circuitry for symmetry. Namely, the gate and the source of Q_6 are connected to the drain of Q_2 and to the gate of Q_4, respectively. Also, the gate of Q_7 is connected to the drain of Q_5. Thereby, it omits the need of extra bias voltages for both NMOS/PMOS modified cascode circuits.

Since the gate voltage (V_{G2}) of Q_2 and the drain voltage (V_{D4}) of Q_4 maintain the value of V_{GS} (=V_{tn} + $V_{OV,n}$), the minimum drain voltage