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Investigation of temperature dependent negative capacitance in the forward bias C-V characteristics of (Au/Ti)/Al_2O_3/n-GaAs Schottky barrier diodes (SBDs)

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ABSTRACT

In this study, a metal-insulator-semiconductor (MIS) type Schottky barrier diodes (SBDs) were fabricated by growing a thin Al_2O_3 insulator layer between Au/Ti and *n*-GaAs using atomic layer deposition (ALD) method. The effect of temperature and voltage on interface states (N_{ss}) and series resistance (R_s) of the (Au/Ti)/Al_2O_3/*n*-GaAs (MIS) type Schottky barrier diodes (SBDs) was investigated using the capacitance/conductance-voltage (*C/(G/ω)-V*) data measured in wide range of temperature (200–380 K) and voltage (± 5 V). It was found that *C* and *G/ω* are strongly dependent on temperature and voltage. The value of C in the forward bias region reaches to maximum and then becomes negative. This negative capacitance (NC) behavior of this SBD is observed for each temperature level. Also, capacitance-current (C-I) and conductance-current (G/ω-I) plots were drawn to explain the NC behavior. The negative value of C in the accumulation region corresponds to the maximum value of G/ω. Such behavior of *C* can be explained by the loss of interface charges located at (Al_2O_3)/n-GaAs interface because of impact ionization process, the existence of surface states (N_{ss}), series resistance (R_s) and interfacial of (Al_2O_3) oxide layer.Therefore, the voltage dependent profiles of R_s and N_{ss} were obtained using Nicollian-Brews and Hill-Colleman methods for enough high forward biases as a function of temperature at various positive bias voltages. The changes in R_s and N_{ss} values were attributed to restructure and reordering of the carriers under temperature and voltage effects.

1. Introduction

Metal-semiconductor (MS) structures with and without thin insulator film have great significance for the research areas that include semiconductor surface studies and electrical characterization studies. These structures are substantially influenced by the production processes, the thickness of insulator layer and its homogeneity and the continuous distribution of N_{ss} at M/S contact. Usually, the *C-V* and *G/ω-V* characteristics are independent of frequency especially at high frequencies and the values of C and G increase with increasing applied bias voltage in the ideal case. However, this case is considerably different in the applications.

The variation in *C* and *G/ω* with applied bias voltage and temperature is especially dependent on the ability of N_{ss} to follow the external ac signal, R_s of the structure, the interfacial insulator layer at M/S interface, and impact ionization or polarization process [1–9]. In other words, different reasons can cause a deviation from ideal behavior such as N_{ss} with different lifetime (τ), R_s, interfacial layer and ionization or polarization [1–15]. For this reason, it is important to take them in account while determining the electrical and dielectric properties. It is well known, the performance of diodes are greatly affected by important factors such as thickness of the thin film at M/S interface, its homogeneity and the barrier formation at M/S interface [7,14–17]. Ionization is an important charge generation mechanism. This process occur when one energetic charge loses energy by the creation of another in a structure. At high temperatures, electrons at M/S interface occupy the vacuous states at the interface when the device is under forward bias but they have redundant energy when they collide with the electrons trapped at the N_{ss}. If the binding energy of these states is lower than the BH energy, they also knock electrons out of the surface states. Therefore N_{ss} is an important device parameters that needs special attention. Various methods can be used to calculate the values of N_{ss} and R_s [1–4,18–21]. While the value of R_s is effective in the accumulation region, the effect of N_{ss} is prominent in depletion and

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reverse bias regions.

The thickness of interlayer and its homogeneity, doping concentration atoms, surface preparation of semiconductor, and the form of BH at M/S interface, frequency, sample temperature and radiation also quite effective on the conduction mechanisms. Lately, some studies have reported negative capacitance phenomena (NC) and eccentric peaks at accumulation region in the *C-V* plots for various semiconductor devices such as MS type SBDs [22,23], hetero-junctions [24,25], some detectors [26–28], MPS type SBDs [14] and Au/1% graphene (GP) doped-$Ca_{1.9}Pr_{0.1}Co_4O_x$/n-Si structures [13]. The use of high-dielectric interfacial layer such as Al_2O_3, TiO_2, $Bi_4Ti_3O_{12}$ (BTO) and graphene-doped PVA at M/S interface enhances the performance, quality and reliability of the MS structures. Therefore, these materials are expected to take the place of the traditional/conventional SiO_2. The use of such high-dielectric materials offers high capacitance, reduced leakage current and enhanced energy capture and storage ability. While the SiO_2 insulator layer formed on a semiconductor by the traditional methods cannot completely passivate the active dangling bonds on the surface of semiconductor, a high-dielectric interfacial layer can decrease the amount of active dangling bonds and so leads to a decrease in the leakage current, surface states (N_{ss}) and series resistance (R_s) while it increases of barrier height (BH). Especially, Al_2O_3 is the most stable and robust oxide that is widely studied in for its suitability for various application areas and it has some interesting properties like dielectric permittivity of ~ 9, wide band gap of ~ 6.6 eV [29–33]. In addition, it has kinetic and thermodynamic stability even at high temperatures and low bulk defect density and it is amorphous under the conditions of interest [33]. Due to the excellent properties of Al_2O_3, it becomes a significant interfacial material and so it may be good alternative to replace the conventional SiO_2 for reducing number of oxygen vacancies and the density of N_{ss}, and for increasing the charge or energy storage and BH at M/S interface. Therefore, in present study, Al_2O_3 thin film was used as an interlayer to reduce the effects of the natural oxide defects like oxygen vacancies and defects like grain boundaries on the electrical and dielectric characteristics of MIS structures.

In our previous search [29], we investigated the temperature dependence of the forward and reverse bias I-V characteristics of the (Au/Ti)/Al_2O_3/*n*-GaAs (MIS) type SBDs. Experimental results revealed that the semi-logarithmic I-V plot for each temperature has two linear regions with different slopes indicating low and intermediate bias voltages which can be clarified by two parallel-diodes model. High values of *n* and low values of BH particularly at low temperatures were felicitously clarified according to the presence of a Gaussian Distribution (GD) of BHs around the mean value of BH because of the BH inhomogeneity between (Au/Ti) and *n*-GaAs layers. Therefore, in present study, the forward and reverse bias C–V-T and G/ω-V-T characteristics of this SBD were investigated in wide range of temperature (200–380 K) and voltage (± 5 V). Eventually, C and G were found to be affected by temperature and voltage. The plot of C-V in the forward bias region reached a maximum value and then took negative values in the strong accumulation region for each temperature level. Moreover, the values of C and G/ω were plotted against current (I) in order to explain the NC behavior. We observed that the negative value of C in the accumulation region agrees to the maximum value of G/ω.

2. Experimental method

(Au/Ti)/Al_2O_3/*n*-GaAs (MIS) structure was fabricated on *n*-GaAs with (100) surface orientation, 380 μm thicknesses, 6.8×10^{15} cm^{-3} doping concentration (N_D). Firstly, *n*- GaAs wafer was cleaned in the ultrasonic bath at various chemical solutions, rinsed in deionized water (DIW) with high resistivity and dried under N_2 gas flow. Secondly, indium with (99.999%) purity and thickness of 2000 Å was coated on the back of n-GaAs at 10^{-6} Torr and then it was annealed at 385 °C for 3 min in N_2 to get ohmic contact with low resistivity. Thirdly, the Al_2O_3 thin film layer was deposited by the ALD method with a growth rate of ~ 1.05 Å per cycle. Finally, the Au (90 nm)/Ti (10 nm) Schottky contacts were formed as dots on the Al_2O_3 with 0.01 cm^2 area. The measurements were held by using an HP-4192 A LF impedance analyzer in the temperature range of 200–380 K at 1 MHz. These measurements were obtained in Janis vpf-475 cryostat by using a Lake Shore model 321 auto-tuning temperature controllers by using of a microcomputer through an IEEE-488 AC/DC converter card. Further details of manufacturing processes and schematic of the samples can be found in our previous search [29].

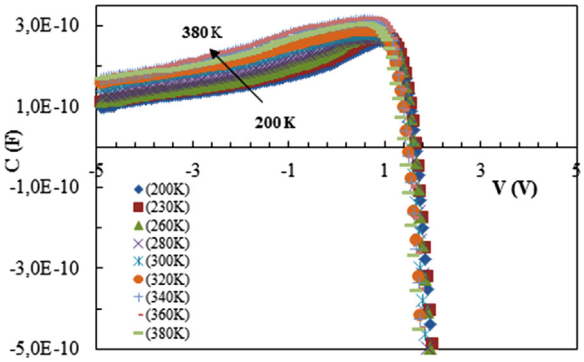

Fig. 1. The variation of the C-V characteristics of the (Au/Ti)/Al_2O_3/*n*-GaAs (MIS) structure at 1 MHz for various temperatures.

3. Results and discussion

It is well know that the main electrical and dielectric characteristics of MIS type structure or capacitors are affected by temperature, interfacial layer and its homogeneity, frequency, the applied voltage or electric field, the formation of barrier height at M/S contact and R_s of them. Therefore, the *C-V* and *G/ω-V* measurements of the (Au/Ti)/Al_2O_3/*n*-GaAs (MIS) structure are held in the temperature range of 200–380 K and at 1 MHz and represented in Figs. 1 and 2, respectively. As shown in Figs. (1) and (2), both C-V and G/ω-V characteristics especially in inversion and accumulation regions reveal noticeable changes with temperature as well as with voltage. As shown in Fig. 3(a-c), while the value of C decreases with increasing temperature for each bias voltage in accumulation region, that of G/w increases. At high temperatures, more and more electronic charges (n), i.e. electron and holes, can gained enough energy to stimulate the conduction and so this leads to an increase in the conductivity (σ = qμn) in conduction band due to the reduction of the forbidden band gap of semiconductor (E_g) with increasing temperature.

The existence of N_{ss} and surface or dipole (oriental) polarization causes a contribution to the values of *C* and *G/ω* at low and

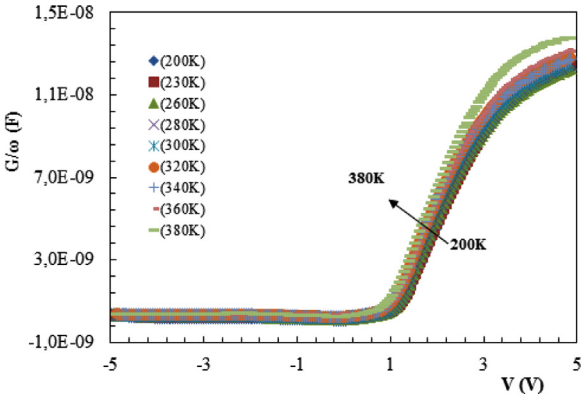

Fig. 2. The variation of the G/ω-V characteristics of the (Au/Ti)/Al_2O_3/*n*-GaAs (MIS) structure at 1 MHz for various temperatures.